S3C2410X LCD 控制器

----文章来源：S3C2410X 用户手册 LCD Controller 部分 作者：三星公司

1 OVERVIEW

1、概述

The LCD controller in the S3C2410X consists of the logic for transferring LCD image data from a video buffer located in system memory to an external LCD driver.

S3C2410X 中的 LCD 控制器由传送逻辑构成，这种逻辑是把位于系统内存显示缓冲区中 LCD 视频数据传到外部的 LCD 驱动器。

The LCD controller supports monochrome, 2-bit per pixel (4-level gray scale) or 4-bit per pixel (16-level gray scale) mode on a monochrome LCD, using a time-based dithering algorithm and Frame Rate Control (FRC) method and it can be interfaced with a color LCD panel at 8-bit per pixel (256-level color) and 12-bit per pixel (4096-level color) for interfacing with STN LCD.
It can support 1-bit per pixel, 2-bit per pixel, 4-bit per pixel, and 8-bit per pixel for interfacing with the palettized TFT color LCD panel, and 16-bit per pixel and 24-bit per pixel for non-palettized true-color display.

LCD 控制器支持单色，使用基于时间的抖动算法和帧频控制的方法，可以支持每像素 2 位（四级灰度）或每像素 4 位（16 级灰度）的单色 LCD 显示屏。也支持彩色 LCD 接口，可以是每像素 8 位（256 种颜色）和每像素 12 位（4096 种颜色）的 STN LCD。

支持每像素 1 位、2 位、4 位和 8 位带有调色板的 TFT 彩色 LCD 和每像素 16 位与 24 位的无调色板真彩色显示。

The LCD controller can be programmed to support different requirements on the screen related to the number of horizontal and vertical pixels, data line width for the data interface, interface timing, and refresh rate.

根据屏幕的水平与垂直像素数，数据界面的数据宽度，界面时间和自刷新速率，LCD 控制器可以编程以支持各种不同要求的显示屏。

2.FEATURES

2、特点

2.1 STN LCD displays:

— Supports 3 types of LCD panels: 4-bit dual scan, 4-bit single scan, and 8-bit single scan display type

— Supports the monochrome, 4 gray levels, and 16 gray levels

— Supports 256 colors and 4096 colors for color STN LCD panel

— Supports multiple screen size

Typical actual screen size: 640×480, 320×240, 160×160, and others

Maximum virtual screen size is 4Mbytes.

Maximum virtual screen size in 256 color mode: 4096×1024, 2048×2048, 1024×4096, and others

2.1、STN 型 LCD 显示器

－支持 3 种扫描方式：4bit 单扫、4 位双扫和 8 位单扫
－支持单色、4 级灰度和 16 级灰度屏
－支持 256 色和 4096 色彩色 STN 屏
－支持多种屏幕尺寸
应用中典型的屏幕尺寸有 640×480, 320×240, 160×160, 和其它
最大虚拟屏幕尺寸达 4Mbytes
256 色颜色模式下最大虚拟屏幕尺寸：4096×1024, 2048×2048, 1024×4096 及其它

2.2 TFT LCD displays:

— Supports 1, 2, 4 or 8-bpp (bit per pixel) palettized color displays for TFT
— Supports 16-bpp non-palettized true-color displays for color TFT
— Supports 24-bpp non-palettized true-color displays for color TFT
— Supports maximum 16M color TFT at 24bit per pixel mode
— Supports multiple screen size
Typical actual screen size: 640×480, 320×240, 160×160, and others
Maximum virtual screen size is 4Mbytes.
Maximum virtual screen size in 64K color mode: 2048×1024 and others

2.2、TFT 型 LCD 显示屏

－支持 1 位、2 位、4 位和 8 位（每像素）调色板 TFT 显示
－支持 16 位/像素非调色板真彩色 TFT 显示
－支持 24 位/像素非调色板真彩色 TFT 显示
－24 位/像素模式下最大支持 16M 彩色 TFT
－支持多种屏幕尺寸
典型分辩率为 640*480、320*240、160*160 及其它多种规格的 LCD
最大虚拟显示达 4Mbytes。
虚拟显示尺寸在 64K 模式下：2048×1024 及其它

2.3 COMMON FEATURES

The LCD controller has a dedicated DMA that supports to fetch the image data from video buffer located in system memory. Its features also include:
— Dedicated interrupt functions (INT_FrSyn and INT_FiCnt)
— The system memory is used as the display memory.
— Supports Multiple Virtual Display Screen (Supports Hardware Horizontal/Vertical Scrolling)
— Programmable timing control for different display panels
— Supports little and big-endian byte ordering, as well as WinCE data formats
— Supports SEC TFT LCD panel (SAMSUNG 3.5″ Portrait/256K Color/Reflective a-Si TFT LCD)
LTS350Q1-PD1: TFT LCD panel with touch panel and front light unit
LTS350Q1-PD2: TFT LCD panel only

2.3、共同特点

LCD 控制器有一个专用 DMA，它不断从位于系统内存中的显示缓冲区获取视频数据。其特点归纳如下：
— 专用中断功能（INT_FrSyn and INT_FiCnt）
— 使用系统内存作为显存
— 支持多种虚拟显示屏（支持水平/垂直滚屏）
— 对于不同的显示屏，支持可编程定时控制

— 支持小端和大端字节模式以及 WinCE 数据格式

— 支持 SEC TFT LCD 屏（ ）

NOTE

WinCE doesn't support the 12-bit packed data format.

Please check if WinCE can support the 12-bit color-mode.

注意

WinCE 不支持 12 位包数据格式。

请检查 WinCE 是否支持 12 彩色模式

2.4 EXTERNAL INTERFACE SIGNAL

VFRAME/VSYNC/STV: Frame synchronous signal (STN)/vertical synchronous signal(TFT)/SEC TFT signal

VLINE/HSYNC/CPV : Line synchronous pulse signal (STN)/horizontal sync signal (TFT)/SEC TFT signal

VCLK/LCD_HCLK : Pixel clock signal (STN/TFT)/SEC TFT signal

VD[23:0] : LCD pixel data output ports (STN/TFT/SEC TFT)

VM/VDEN/TP : AC bias signal for the LCD driver (STN)/data enable signal (TFT)/SEC TFT signal

LEND/STH : Line end signal (TFT)/SEC TFT signal

LCD_PWREN : LCD panel power enable control signal

LCDVF0 : SEC TFT Signal OE

LCDVF1 : SEC TFT Signal REV

LCDVF2 : SEC TFT Signal REVB

The 33 output ports in total includes 24 data bits and 9 control bits

2.4、外部接口信号

VFRAME/VSYNC/STV ：帧同步信号（STN）/ 垂直同步信号（TFT）/ SEC TFT 信号

VLINE/HSYNC/CPV ：行同步脉冲信号（STN）/ 水平同步信号（TFT）/ SEC TFT 信号

VCLK/LCD_HCLK ：像素时钟信号（STN/TFT）/ SEC TFT 信号

VD[23:0] ：LCD 像素数据输出端口(STN/TFT/SEC TFT)

VM/VDEN/TP ：LCD 驱动器交流信号（STN）/ 数据使能信号（TFT）/ SEC TFT 信号

LEND/STH ：行结束信号(TFT)/SEC TFT 信号

LCD_PWREN ：LCD 屏电源控制信号

LCDVF0 ：SEC TFT 信号 OE

LCDVF1 ：SEC TFT 信号 REV

LCDVF2 ：SEC TFT 信号 REVB

2.4 BLOCK DIAGRAM

2.4、方框图

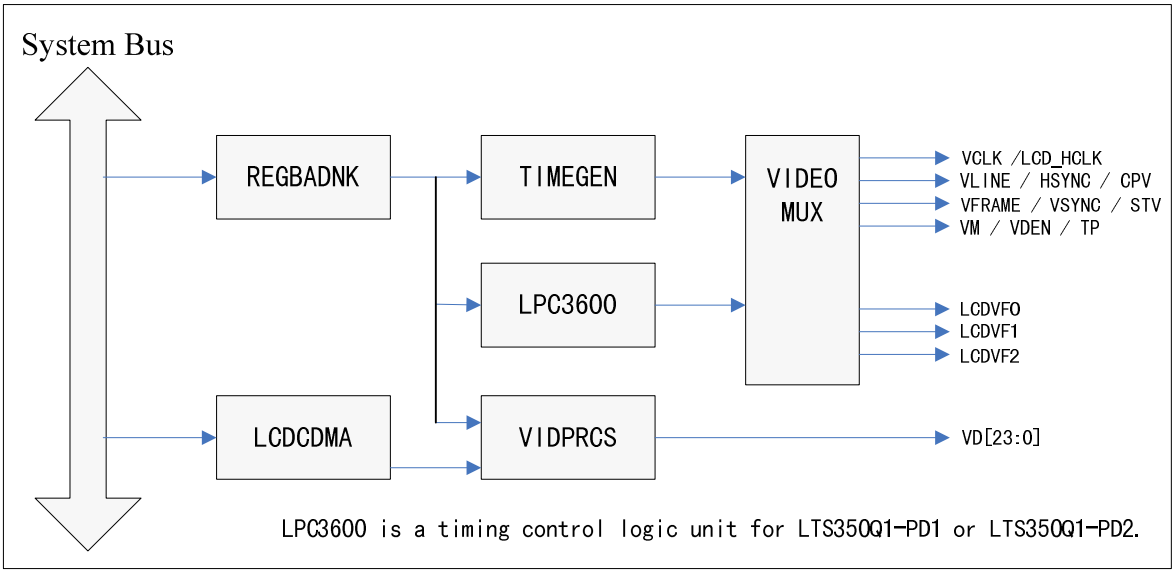


Figure 15-1. LCD Controller Block Diagram

图 15-1 LCD 控制器框图

The S3C2410X LCD controller is used to transfer the video data and to generate the necessary control signals, such as VFRAME, VLINE, VCLK, VM, and so on. In addition to the control signals, the S3C2410X has the data ports for video data, which are VD[23:0] as shown in Figure 15-1. The LCD controller consists of a REGBANK, LCDCDMA, VIDPRCS, TIMEGEN, and LPC3600 (See the Figure 15-1 LCD Controller Block Diagram). The REGBANK has 17 programmable register sets and 256x16 palette memory which are used to configure the LCD controller. The LCDCDMA is a dedicated DMA, which can transfer the video data in frame memory to LCD driver automatically. By using this special DMA, the video data can be displayed on the screen without CPU intervention. The VIDPRCS receives the video data from the LCDCDMA and sends the video data through the VD[23:0] data ports to the LCD driver after changing them into a suitable data format, for example 4/8-bit single scan or 4-bit dual scan display mode. The TIMEGEN consists of programmable logic to support the variable requirements of interface timing and rates commonly found in different LCD drivers. The TIMEGEN block generates VFRAME, VLINE, VCLK, VM, and so on.

S3C2410X 中 LCD 控制器用为传送视频数据和产生需要的控制信号的，如 VFRAME, VLINE, VCLK, VM, 等。除控制信号外，S3C2410X 中的 LCD 控制器还有传送视频数据的端口，如图中 VD[23:0]所示。LCD 控制器由 REGBANK, LCDCDMA, VIDPRCS, TIMEGEN, and LPC3600（如图 15-1 LCD 控制器框图）组成。REGBANK 有 17 个可编程寄存器组和用来配置 LCD 控制器的 256*16 的调色板存储器。LCDCDMA 是一个专用 DMA，自动传送帖数据到 LCD 驱动器。利用这个特殊的 DMA，视频数据可以在没有 CPU 的参与下自动显示。VIDPRCS 从 LCDCDMA 接收视频数据，然后将其转换成适合的数据格式通过数据端口 VD[23:0]发送到 LCD 驱动器上，例如 4/8 位单扫描或 4 位双扫描模式。TIMEGEN 由可编程逻辑组成，支持各种常见 LCD 驱动器的定时与速率界面的不同要求。TIMEGEN 模块产生 FRAME, VLINE, VCLK, VM 等信号。

The description of data flow is as follows:

FIFO memory is present in the LCDCDMA. When FIFO is empty or partially empty, the LCDCDMA requests data fetching from the frame memory based on the burst memory transfer mode (consecutive memory fetching of 4 words (16 bytes) per one burst request without allowing the bus mastership to another bus master during the bus transfer). When the transfer request is accepted by bus arbitrator

in the memory controller, there will be four successive word data transfers from system memory to internal FIFO. The total size of FIFO is 28 words, which consists of 12 words FIFOL and 16 words FIFOH, respectively. The S3C2410X has two FIFOs to support the dual scan display mode. In case of single scan mode, one of the FIFOs (FIFOH) can only be used.

数据流描述如下：

LCDCDMA 有 FIFO（First-In First-Out, 先入先出）存储器。当 FIFO 为空或者部分为空时，LCDCDMA 模块就以爆发式传送模式从帧存储器中取数据（每次爆发式请求连续取 16 个字节，期间不允许总线控制权的转变）。当传送请求被位于内存控制器中的总线仲裁器接受时，将有连续的 4 个字的数据从系统内存送到外部的 FIFO。FIFO 的大小总共为 28 字，其中分别有 12 个字的 FIFOL 和 16 个字的 FIFOH。S3C2410X 有两个 FIFO 存储器以支持双扫描显示模式。在单扫描模式下只有一路 FIFO（FIFOH）工作。

3.STN LCD CONTROLLER OPERATION

3、STN 型 LCD 控制操作

3.1 TIMING GENERATOR (TIMEGEN)

3.1、脉冲发生器（TIMEGEN）

The TIMEGEN generates the control signals for the LCD driver, such as VFRAME, VLINE, VCLK, and VM. These control signals are closely related to the configuration on the LCDCON1/2/3/4/5 registers in the REGBANK.

Based on these programmable configurations on the LCD control registers in the REGBANK, the TIMEGEN can generate the programmable control signals suitable to support many different types of LCD drivers.

TIMEGEN（脉冲发生器）用来产生 LCD 驱动器的控制信号，如 VFRAME、VLINE、VCLK 和 VM。这些控制信号与寄存器组中控制寄存器 LCDCON1/2/3/4/5 的配置密切相关。

基于这些 LCD 控制寄存器的可编程配置，TIMEGEN 就能产生可编程的控制信号，以适合支持多种不同类型的 LCD 驱动器。

The VFRAME pulse is asserted for the duration of the entire first line at a frequency of once per frame. The VFRAME signal is asserted to bring the LCD's line pointer to the top of the display to start over.

以帧为周期，在整个第一行期间，插入一个 VFRAME（帧）脉冲信号。VFRAME 信号使行指针回到显示器的顶行重新开始新的一帧。

The VM signal helps the LCD driver alternate the polarity of the row and column voltages, which are used to turn the pixel on and off. The toggling rate of VM signals depends on the MMODE bit of the LCDCON1 register and MVAL field of the LCDCON4 register. If the MMODE bit is 0, the VM signal is configured to toggle on every frame. If the MMODE bit is 1, the VM signal is configured to toggle on the every event of the elapse of the specified number of VLINE by the MVAL[7:0] value. Figure 15-4 shows an example for MMODE=0 and for MMODE=1 with the value of MVAL[7:0]=0x2. When MMODE=1, the VM rate is related to MVAL[7:0], as shown below:

VM Rate = VLINE Rate / (2 * MVAL)

VM 信号使 LCD 驱动器的行和列电压极性交替变换，用作对像素的开与关。VM 信号的触发速率决定于 LCDCON1 寄存器中 MMODE 位和 LCDCON4 寄存器 MVAL 区的设置。若 MMODE 位为 0，则 VM 信号每帧触发一次。若 MMODE 位为 1，则 VM 信号在指定数量的 VLINE 信号后的触发，VLINE 数量由 MVAL[7：0]的值决定。图 15—4 显示了以 MMODE=0 和 MMODE=1 且 MVAL[7：0]=0x2 时的例子。当 MMODE=1 时，VM 信号的速率与 MVAL[7：0]的值有关，公式为：

VM 速率 = VLINE 速率 / （2 * MVAL）

The VFRAME and VLINE pulse generation relies on the configurations of the HOZVAL field and the LINEVAL field in the LCDCON2/3 register. Each field is related to the LCD size and display mode. In other words, the HOZVAL and LINEVAL can be determined by the size of the LCD panel and the display mode according to the following equation:

HOZVAL = (Horizontal display size / Number of the valid VD data line)-1

In color mode: Horizontal display size = 3 * Number of Horizontal Pixel

VFRAME 和 VLINE 脉冲的产生取决于 LCDCON2/3 寄存器中 HOZVAL 和 LINEVAL 的配置，它们都与 LCD 屏的大小和显示模式有关。换句话说，HOZVAL 和 LINEVAL 可由 LCD 屏与显示模式决定，公式如下：

HOZVAL = （水平显示尺寸/ 有效 VD 数据队列数）-1

彩色显示模式下：水平显示尺寸 = 3 * 水平像素数

In the 4-bit single scan display mode, the Number of valid VD data line should be 4. In case of 4-bit dual scan display, the Number of valid VD data line should also be 4 while in case of 8-bit single scan display mode, the Number of valid VD data line should be 8.

LINEVAL = (Vertical display size) -1: In case of single scan display type

LINEVAL = (Vertical display size / 2) -1: In case of dual scan display type

在 4 位单扫描模式下，有效 VD 数据队列数应为 4。若用 4 位双扫描显示，有效的 VD 数据队列数也应为 4，但在 8 位单扫描模式下，有效的 VD 数据队列数应为 8。

LINEVAL = （垂直显示尺寸）-1 ：单扫描情况

LINEVAL = （垂直显示尺寸 / 2）-1 ：双扫描情况

The rate of VCLK signal depends on the configuration of the CLKVAL field in the LCDCON1 register. Table 15-1 defines the relationship of VCLK and CLKVAL. The minimum value of CLKVAL is 2.

VCLK(Hz)=HCLK/(CLKVAL x 2)

The frame rate is the VFRAM signal frequency. The frame rate is closely related to the field of WLH[1:0](VLINE pulse width) WDLY[1:0] (the delay width of VCLK after VLINE pulse), HOZVAL, LINEBLANK, and LINEVAL in the LCDCON1/2/3/4 registers as well as VCLK and HCLK. Most LCD drivers need their own adequate frame rate. The frame rate is calculated as follows:

frame_rate(Hz) = 1 / [{ (1/VCLK)×(HOZVAL+1)+(1/HCLK) ×(A+B+(LINEBLANK×8)) }×(LINEVAL+1)]

$$A = 2^{(4+WLH)},\ B = 2^{(4+WDLY)}$$

Table 15-1. Relation Between VCLK and CLKVAL (STN, HCLK = 60 MHz)

CLKVAL	60 MHz/X	VCLK
2	60 MHz/4	15.0 MHz
3	60 MHz/6	10.0 MHz
:	:	:
1023	60 MHz/2046	29.3 kHz

VCLK 信号的速率取决于 LCDCON1 寄存器中 CLKVAL 的配置。表 15-1 定义了 VCLK 与 CLKVAL 的关系。CLKVAL 的最小值为 2。

VCLK(Hz)=HCLK/(CLKVAL x 2)

帧频（帧速率）就是 VFRAM 信号的频率。帧频和寄存器 LCDCON1/2/3/4 中 WLH[1：0]（VLINE 脉冲宽

度)、WDLY[1：0]（VCLK 延迟于 VLINE 脉冲的宽度)、HOZVAL、LINEBLANK 和 LINEVAL 及 VCLK 和 HCLK 密切相关。大多数 LCD 驱动器有它们适合帧频。帧频可由下列公式计算得出：

帧频(Hz) = 1/[{ (1/VCLK)×(HOZVAL+1)+(1/HCLK)×(A+B+(LINEBLANK×8))}×(LINEVAL+1)]

$$A = 2^{(4+WLH)},\ B = 2^{(4+WDLY)}$$

4 VIDEO OPERATION

4、视频操作

The S3C2410X LCD controller supports 8-bit color mode (256 color mode), 12-bit color mode (4096 color mode), 4 level gray scale mode, 16 level gray scale mode as well as the monochrome mode. For the gray or color mode, it is required to implement the shades of gray level or color according to time-based dithering algorithm and Frame Rate Control (FRC) method. The selection can be made following a programmable lockup table, which will be explained later. The monochrome mode bypasses these modules (FRC and lookup table) and basically serializes the data in FIFOH (and FIFOL if a dual scan display type is used) into 4-bit (or 8-bit if a 4-bit dual scan or 8-bit single scan display type is used) streams by shifting the video data to the LCD driver.

The following sections describe the operation on the gray and color mode in terms of the lookup table and FRC.

S3C2410X 的 LCD 控制器可支持 8 位彩色模式（256 色模式)，12 位彩色模式（4096 色模式)，4 级灰度模式，16 级灰度模式以及单色模式。对于灰度或彩色模式，需要基于时间抖动和帧速率控制的方法来实现灰度或彩色的分级。可以通过一个可编程的查找表选择，这个以后会作解释。单色模式则不需要这些模块（FRC 和查找表)，基本上通过转换视频数据使 FIFOH（如果是双扫描显示类型则还有 FIFOL）的数据串行化为 4 位（若为 4 位双扫描或 8 位单扫描显示类型时为 8 位）数据流到 LCD 驱动器。

接下来的部分将介绍根据查找表和 FRC 在灰度和彩色模式下的操作。

Lookup Table

The S3C2410X can support the lookup table for various selection of color or gray level mapping, ensuring flexible operation for users. The lookup table is the palette which allows the selection on the level of color or gray (Selection on 4-gray levels among 16 gray levels in case of 4 gray mode, selection on 8 red levels among 16 levels, 8 green levels among 16 levels and 4 blue levels among 16 levels in case of 256 color mode). In other words, users can select 4 gray levels among 16 gray levels by using the lookup table in the 4 gray level mode. The gray levels cannot be selected in the 16 gray level mode; all 16 gray levels must be chosen among the possible 16 gray levels. In case of 256 color mode, 3 bits are allocated for red, 3 bits for green and 2 bits for blue. The 256 colors mean that the colors are formed from the combination of 8 red, 8 green and 4 blue levels (8x8x4 = 256). In the color mode, the lookup table can be used for suitable selections. Eight red levels can be selected among 16 possible red levels, 8 green levels among 16 green levels, and 4 blue levels among 16 blue levels. In case of 4096 color mode, there is no selection as in the 256 color mode.

查找表

S3C2410X 能支持多样选择的颜色或灰度映射的颜色查找表，确保用户使用弹性化。颜色查找表是可以选择彩色或灰度级别（在 4 级灰度模式下可选择 16 级灰度中的 4 级，在 256 色模式下可选择 16 级红色中的 8 种，16 级绿色中的 8 种和 16 级蓝色中的 4 种）的调色板。换句话说就是，在 4 级灰度模式下，利用查找表用户可以选择 16 级灰度中的 4 级。在 16 级灰度模式下，灰度级别是不能选择的。在可能的 16 级

灰度中所有的 16 种灰度必须选择。在 256 色模式下，3 位代表红色，3 位代表绿色，2 位代表蓝色。这 256 种颜色是指由 8 种红色、8 种绿色和 4 种蓝色（8*8*8=256 种）组合而成的。在其它模式下，查找表可适当选择。8 种红色可从 16 级红色选择，8 种绿色可从 16 级绿色选择，4 种蓝色可从 16 级蓝色选择。在 4096 色模式下不能像在 256 色模式下那样选择。

5 Gray Mode Operation

5、灰度模式操作

The S3C2410X LCD controller supports two gray modes: 2-bit per pixel gray (4 level gray scale) and 4-bit per pixel gray (16 level gray scale). The 2-bit per pixel gray mode uses a lookup table (BLUELUT), which allows selection on 4 gray levels among 16 possible gray levels. The 2-bit per pixel gray lookup table uses the BULEVAL[15:0] in Blue Lookup Table (BLUELUT) register as same as blue lookup table in color mode. The gray level 0 will be denoted by BLUEVAL[3:0] value. If BLUEVAL[3:0] is 9, level 0 will be represented by gray level 9 among 16 gray levels. If BLUEVAL[3:0] is 15, level 0 will be represented by gray level 15 among 16 gray levels, and so on. Following the same method as above, level 1 will also be denoted by BLUEVAL[7:4], the level 2 by BLUEVAL[11:8], and the level 3 by BLUEVAL[15:12]. These four groups among BLUEVAL[15:0] will represent level 0, level 1, level 2, and level 3. In 16 gray levels, there is no selection as in the 16 gray levels.

S3C2410X 的 LCD 控制器支持 2 种灰度模式：每像素 2 位灰色（4 级灰度）和每像素 4 位灰色（16 级灰度）。2 位/像素灰色模式下使用一个查找表（BLUELUT），允许在 16 级可能的灰度中选择 4 种。2 位/像素灰色查找表用的是蓝色查找表（BLUELUT）寄存器中 BLUEVAL[15：0]，就像在彩色模式下的使用蓝色查找表一样。0 级灰度由 BLUEVAL[3:0]指定。若 BLUEVAL[3:0]值为 9，则 0 级灰度就代表 16 级灰度中的第 9 级灰度。若 BLUEVAL[3:0]值为 15，则 0 级灰度就代表 16 级灰度中的第 15 级灰度，如此类推。按上面介绍的方法，1 级灰度由 BLUEVAL[7：4]指定，2 级灰度由 BLUEVAL[11：8]指定而 3 级灰度就由 BLUEVAL[15：12]指定。BLUEVAL[15：0]中这四组值就分别代表灰度 0、灰度 1、灰度 2 和灰度 3。在 16 级灰度模式下就不需要选择了。

6.256 Level Color Mode Operation

6、256 级彩色模式操作

The S3C2410X LCD controller can support an 8-bit per pixel 256 color display mode. The color display mode can generate 256 levels of color using the dithering algorithm and FRC. The 8-bit per pixel are encoded into 3-bits for red, 3-bits for green, and 2-bits for blue. The color display mode uses separate lookup tables for red, green, and blue. Each lookup table uses the REDVAL[31:0] of REDLUT register, GREENVAL[31:0] of GREENLUT register, and BLUEVAL[15:0] of BLUELUT register as the programmable lookup table entries.

S3C2410X 的 LCD 控制器可支持 8 位/像素的 256 色显示模式。利用抖动算法和帧频控制，彩色显示模式下可产生 256 种颜色。每像素的 8 位可编码成为 3 位代表红色、3 位代表绿色和位代表蓝色。彩色显示模式使用单独的红色、绿色和蓝色查找表。它们分别用寄存器 REDLUT 中 REDVAL[31：0]、寄存器 GREENLUT 中 GREENVAL[31：0]和寄存器 BLUELUT 中 BLUEVAL[15：0]作为可编程的查找表项。

Similar to the gray level display, 8 group or field of 4 bits in the REDLUR register, i.e., REDVAL[31:28], REDLUT[27:24], REDLUT[23:20], REDLUT[19:16], REDLUT[15:12], REDLUT[11:8], REDLUT[7:4], and REDLUT[3:0], are assigned to each red level. The possible combination of 4 bits

(each field) is 16, and each red level should be assigned to one level among possible 16 cases. In other words, the user can select the suitable red level by using this type of lookup table. For green color, the GREENVAL[31:0] of the GREENLUT register is assigned as the lookup table, as was done in the case of red color. Similarly, the BLUEVAL[15:0] of the BLUELUT register is also assigned as a lookup table. For blue color, 2 bits are allocated for 4 blue levels, different from the 8 red or green levels.

和灰度显示一样，寄存器 REDLUT 可 8 组每组 4 位，也就是 REDVAL[31:28]、REDLUT[27:24]、REDLUT[23:20]、REDLUT[19:16]、REDLUT[15:12]、REDLUT[11:8]、REDLUT[7:4]和 REDLUT[3:0]，分别指定一种红色级别。每组中的 4 位的可能组合数为 16，每种红色级别应指定为 16 种可能级别中的一种。换言之，用户利用这种查找表可以选择适合的红色级别。对于绿色，寄存器 GREENLUT 中的 GREENVAL[31：0]作为查找表，和红色查表作同样的处理。同样地，寄存器 BLUELUT 中 BLUEVAL[15：0]也被指派为查找表。对于蓝色，和 8 级红色或绿色级别不同，只有 2 位，可以指定 4 级蓝色。

6. 4096 Level Color Mode Operation

6、4096 级彩色模式操作

The S3C2410X LCD controller can support a 12-bit per pixel 4096 color display mode. The color display mode can generate 4096 levels of color using the dithering algorithm and FRC. The 12-bit per pixel are encoded into 4- bits for red, 4-bits for green, and 4-bits for blue. The 4096 color display mode does not use lookup tables.

S3C2410X 的 LCD 控制器可以支持 12 位/像素的 4096 色显示模式。利用抖动算法和帧频控制，这种彩色显示模式可产生 4096 种颜色。代表一个像素的 12 位编码为 4 位代表红色、4 位代表绿色和 4 位代表蓝色。4096 色显示模式下不使用颜色查找表。

DITHERING AND FRAME RATE CONTROL

抖动和帧频控制

For STN LCD displays (except monochrome), video data must be processed by a dithering algorithm. The DITHFRC block has two functions, such as Time-based Dithering Algorithm for reducing flicker and Frame Rate Control (FRC) for displaying gray and color level on the STN panel. The main principle of gray and color level display on the STN panel based on FRC is described. For example, to display the third gray (3/16) level from a total of 16 levels, the 3 times pixel should be on and 13 times pixel off. In other words, 3 frames should be selected among the 16 frames, of which 3 frames should have a pixel-on on a specific pixel while the remaining 13 frames should have a pixel-off on a specific pixel. These 16 frames should be displayed periodically. This is basic principle on how to display the gray level on the screen, so-called gray level display by FRC. The actual example is shown in Table 15-2. To represent the 14th gray level in the table, we should have a 6/7 duty cycle, which mean that there are 6 times pixel-on and one time pixel-off. The other cases for all gray levels are also shown in Table 15-2.

对于 STN 型 LCD 显示屏（单色除外），视频数据都必须经过抖动算法的处理。DITHFRC 有两个功能，如为减少闪烁而设的基于时间的抖动算法和为在 STN 型屏上显示灰色或彩色的帧频控制。在 STN 型屏上基于帧频控制的灰色或彩色显示原理这里将作介绍。例如，为了显示总共 16 级灰度中的第 3 级灰度（3/16），显示的像素需要开 3 个时间单位而关闭 13 个时间单位。换言之，在 16 帧数据中，一个特定的像素在 3 帧中是显示的，而在其它 13 帧中这一像素是不显示的。这 16 帧数据是周期性地被显示的。这是在显示屏上显示灰度的一个基本原理，即所谓的基于帧频控制的灰度显示。实际例子见表 15-2 所示。如表中代表 14 级灰度的，需要一个 6/7 的占空比，即 6 个单位时间像素显示而一个单位时间像素不显示。其它所有灰度

显示的情况见表 15-2。

In the STN LCD display, we should be reminded of one item, i.e., Flicker Noise due to the simultaneous pixel-on and -off on adjacent frames. For example, if all pixels on first frame are turned on and all pixels on next frame are turned off, the Flicker Noise will be maximized. To reduce the Flicker Noise on the screen, the average probability of pixel-on and -off between frames should be the same. In order to realize this, the Time-based Dithering Algorithm, which varies the pattern of adjacent pixels on every frame, should be used. This is explained in detail. For the 16 gray level, FRC should have the following relationship between gray level and FRC. The 15th gray level should always have pixel-on, and the 14th gray level should have 6 times pixel-on and one times pixel-off, and the 13th gray level should have 4 times pixel-on and one times pixel-off, ,,,,,,,, , and the 0th gray level should always have pixel-off as shown in Table 15-2.

使用 STN 型 LCD 时，我们应注意一项，也就是，闪变噪声是由于邻近的帧中的像素同时开与关。例如，若第一帧中所有的像素都是开的，而下一帧的所的像素都是关的，闪变噪声将会达到最大。为了减少屏上的闪变噪声，像素开与关的的概率应相近。为了实现这一点，可使用基于时间的抖动算法，它可以使每帧中邻近的像素样式更多样化。下面是详细的说明。对于 16 级灰度，帧频控制应有以下灰度级别和帧频控制间的关系。第 15 级灰度应该使像素保持开状态，第 14 级灰度应有 6 个单们时间是开的和 1 个单位的时间是关的，第 13 级灰度应使 4 个单位时间开和 1 个单位时间关，……，而第 0 级灰度应使像素始终是关的，见表 15-2。

Table 15-2. Dither Duty Cycle Examples

Pre-Dithered Data (gray level number)	Duty Cycle	Pre-Dithered Data (gray level number)	Duty Cycle
15	1	7	1/2
14	6/7	6	3/7
13	4/5	5	2/5
12	3/4	4	1/3
11	5/7	3	1/4
10	2/3	2	1/5
9	3/5	1	1/7
8	4/7	0	0

Display Types

显示类型

The LCD controller supports 3 types of LCD drivers: 4-bit dual scan, 4-bit single scan, and 8-bit single scan display mode. Figure 15-2 shows these 3 different display types for monochrome displays, and Figure 15-3 show these 3 different display types for color displays.

LCD 控制器支持 3 种类型的 LCD 驱动器：4 位双扫描、4 位单扫描和 8 位单扫描显示模式。图 15-2 为单色显示下的三种显示类型。图 15-3 为在彩色显示方式下的三种显示类型。

.1 4-bit Dual Scan Display Type

A 4-bit dual scan display uses 8 parallel data lines to shift data to both the upper and lower halves of the display at the same time. The 4 bits of data in the 8 parallel data lines are shifted to the upper half and 4 bits of data is shifted to the lower half, as shown in Figure 15-2. The end of frame is reached when each half of the display has been shifted and transferred. The 8

pins (VD[7:0]) for the LCD output from the LCD controller can be directly connected to the LCD driver.

.1、四位双扫描显示方式

4 位双扫描用 8 位并行数据线同时移送数据至显示屏的上半屏和下半屏。8 个平行数据线中有 4 位数据被移入上半屏，而另一半被移入下半屏，如图 15-2 所示。当每个半屏中数据移送完毕时一帧便结束。LCD 控制器引出的 8 个 LCD 输出端（VD[7：0]）可直接与 LCD 驱动器相连。

4-bit Single Scan Display Type

A 4-bit single scan display uses 4 parallel data lines to shift data to successive single horizontal lines of the display at a time, until the entire frame has been shifted and transferred. The 4 pins (VD[3:0]) for the LCD output from the LCD controller can be directly connected to the LCD driver, and the 4 pins (VD[7:4]) for the LCD output are not used.

4 位单扫描显示方式

4 位单扫描采用 4 位并行数据线将行数据一次连续移出，直到整个帧的数据被移出为止。从 LCD 控制器引出的 4 个 LCD 输出端（VD[3：0]）可直接连到 LCD 驱动器上，而 LCD 输出端的另 4 个端口（VD[7：4]）则没用。

8-bit Single Scan Display Type

An 8-bit single scan display uses 8 parallel data lines to shift data to successive single horizontal lines of the display at a time, until the entire frame has been shifted and transferred. The 8 pins (VD[7:0]) for the LCD output from the LCD controller can be directly connected to the LCD driver.

8 位单扫描显示方式

8 位单扫描采用 8 位并行数据线将行数据一次连续移出，直到整个帧的数据被移出为止。从 LCD 控制器引出的 8 个 LCD 输出端（VD[7：0]）可直接连到 LCD 驱动器上

256 Color Displays

Color displays require 3 bits (Red, Green, and Blue) of image data per pixel, and so the number of horizontal shift registers for each horizontal line corresponds to three times the number of pixels of one horizontal line. Resulting in a horizontal shift register of length 3 times the number of pixels per horizontal line . This RGB is shifted to the LCD driver as consecutive bits via the parallel data lines. Figure 15-3 shows the RGB and order of the pixels in the parallel data lines for the 3 types of color displays.

256 色显示方式

彩色显示下每个像素的图像数据需要 3 位（红绿蓝），即每行的移位寄存器数量相当于 3 倍的水平像素数。所以一个水平移位寄存器的长度是行像素数量的 3 倍。RGB 数据以连续的位数据通过并行线移位至 LCD 驱动器。 如图 15-3 所示，在三种显示方式下，像素在并行数据线中的三种颜色和顺序。

4096 Color Displays

4096 色显示方式

Color displays require 3 bits (Red, Green, and Blue) of image data per pixel, and so the number of horizontal shift registers for each horizontal line corresponds to three times the number of pixels of one horizontal line. This RGB is shifted to the LCD driver as consecutive bits via the parallel data lines. This RGB order is determined by the sequence of video data in video buffers.

三种颜色的顺序决定于显示缓冲区中视频数据的次序。

MEMORY DATA FORMAT (STN, BSWP=0) 内存中的数据格式

Mono 4-bit Dual Scan Display: 单色 4 位双扫描显示

Video Buffer Memory:（视频缓冲区）

Address（地址）	Data（数据）
0000H	A[31:0]
0004H	B[31:0]
•	
•	
•	
1000H	L[31:0]
1004H	M[31:0]
•	
•	
•	

LCD Panel

A[31] A[30] ..... A[0] B[31] B[30] ..... B[0] .....

L[31] L[30] ..... L[0] M[31] M[30] ..... M[0] .....

Mono 4-bit Single Scan Display & 8-bit Single Scan Display:

(单色 4 位单扫描和 8 位单扫描)

Video Buffer Memory:

Address（地址）	Data（数据）
0000H	A[31:0]
0004H	B[31:0]
0008H	C[31:0]
•	
•	
•	

LCD Panel

A[31] A[30] A[29] ..... A[0] B[31] B[30] ..... B[0] C[31] ..... C[0] .....

MEMORY DATA FORMAT (STN, BSWP=0) (CONTINUED)

In 4-level gray mode, 2 bits of video data correspond to 1 pixel.

In 16-level gray mode, 4 bits of video data correspond to 1 pixel.

In 256 level color mode, 8 bits (3 bits of red, 3 bits of green, and 2 bits of blue) of video data correspond to 1 pixel. The color data format in a byte is as follows:

Bit [7:5]	Bit [4:2]	Bit[1:0]
Red	Green	Blue

In 4096 level color mode, 12 bits (4 bits of red, 4 bits of green, 4 bits of blue) of video data correspond to 1 pixel.The following table shows color data format in words: (Video data must reside at 3 word boundaries (8 pixel), as follows)

RGB Order

DATA	[31:28]	[27:24]	[23:20]	[19:16]	[15:12]	[11:8]	[7:4]	[3:0]
Word #1	Red(1)	Green(1)	Blue(1)	Red(2)	Green(2)	Blue(2)	Red(3)	Green(3)
Word #2	Blue(3)	Red(4)	Green(4)	Blue(4)	Red(5)	Green(5)	Blue(5)	Red(6)
Word #3	Green(6)	Blue(6)	Red(7)	Green(7)	Blue(7)	Red(8)	Green(8)	Blue(8)

内存中数据的格式（STN, BSWP=0）

4 级灰度模式下，一个像素由 2 位视频数据表示。

16 级灰度模式下，一个像素由 4 位视频数据表示。

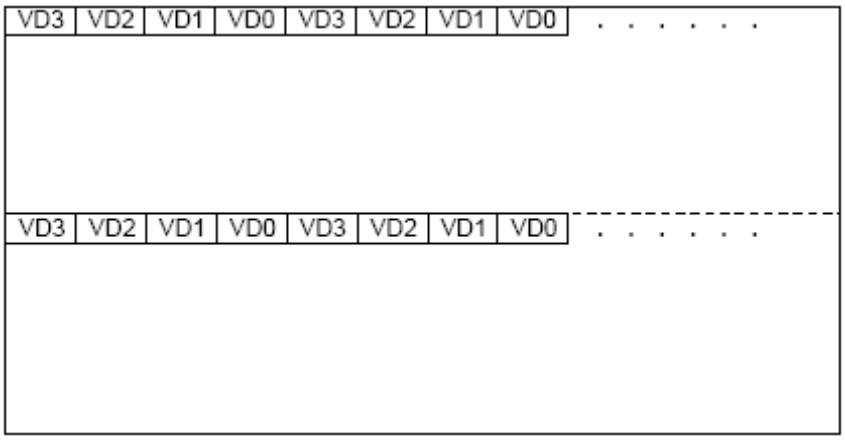
256 级彩色模式下，一个像素由 8 位（其中 3 位红色，3 位绿色，2 位蓝色）视频数据表示，彩色数据格式如下表所示：

位[7:5]	位[4:2]	位[1:0]
红	绿	蓝

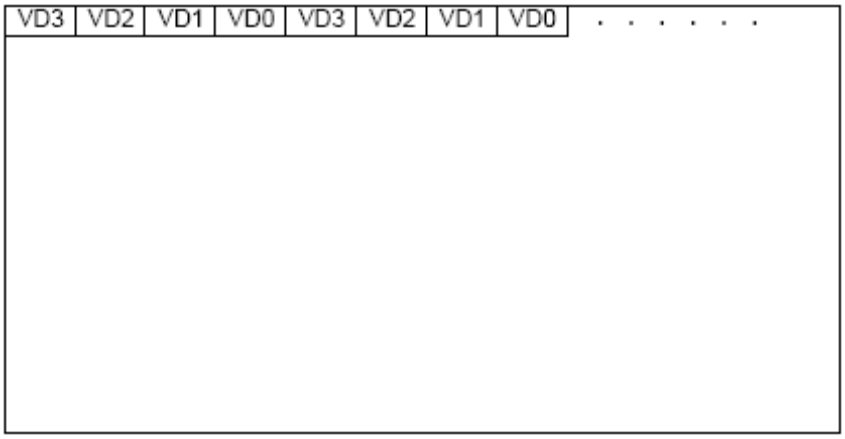
4096 级彩色模式下，一个像素由 12 位（其中 4 位红色，4 位绿色，4 位蓝色）视频数据表示。下表表示了字内彩色数据格式（如下：视频数据必须以三个字为界）。

RGB 顺序

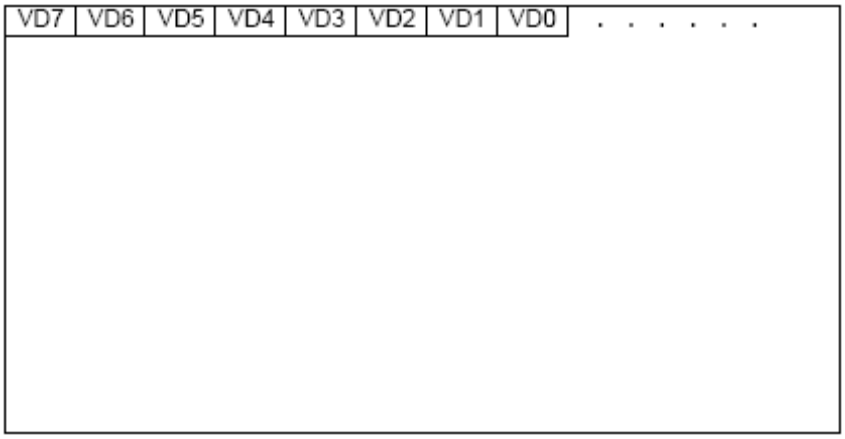
数据	[31:28]	[27:24]	[23:20]	[19:16]	[15:12]	[11:8]	[7:4]	[3:0]
字 #1	红(1)	绿(1)	蓝(1)	红(2)	绿(2)	蓝(2)	红(3)	绿(3)
字 #2	蓝(3)	红(4)	绿(4)	蓝(4)	红(5)	绿(5)	蓝(5)	红(6)
字 #3	绿(6)	蓝(6)	红(7)	绿(7)	蓝(7)	红(8)	绿(8)	蓝(8)



4-bit Dual Scan Display（4 位双扫描显示）



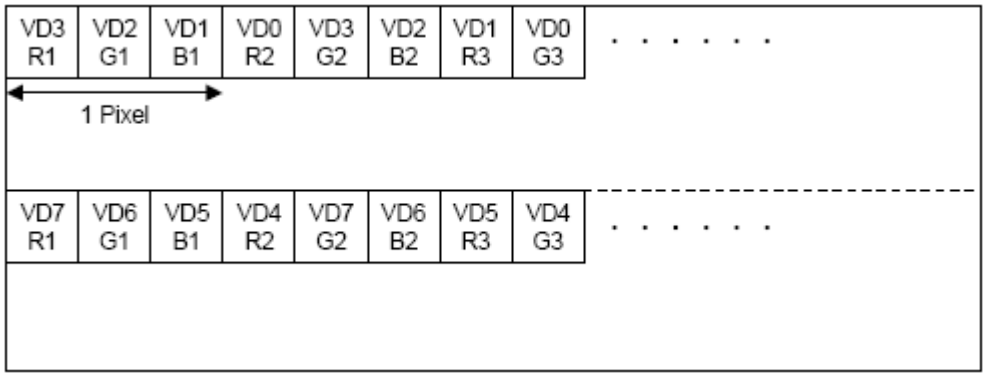
4-bit Single Scan Display（4 位单扫描显示）



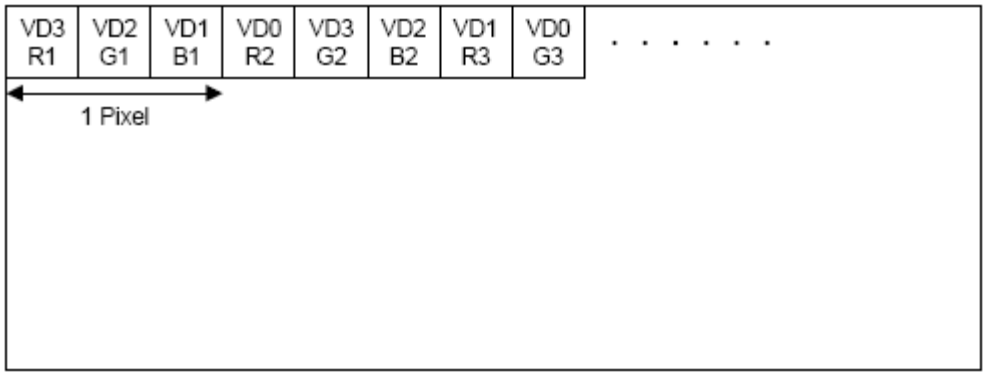
8-bit Single Scan Display（8 位单扫描显示）

Figure 15-2. Monochrome Display Types (STN)

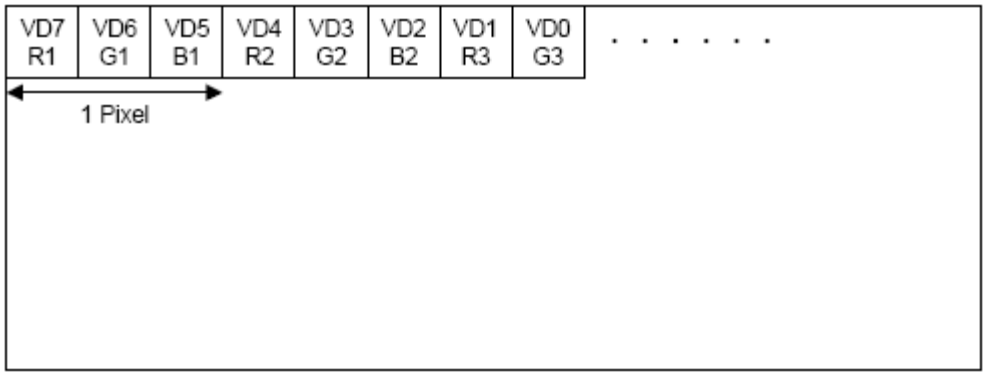
图 15-2 单色显示(STN)



4-bit Dual Scan Display（4 位双扫描显示）



4-bit Single Scan Display（4 位单扫描显示）



8-bit Single Scan Display（8 位单扫描显示）

Figure 15-3. Color Display Types (STN)

图 15-3 彩色显示(STN)

Timing Requirements

Image data should be transferred from the memory to the LCD driver using the VD[7:0] signal. VCLK signal is used to clock the data into the LCD driver's shift register. After each horizontal line of data has been shifted into the LCD driver's shift register, the VLINE signal is asserted to display the line on the panel.

The VM signal provides an AC signal for the display. The LCD uses the signal to alternate the polarity of the row and column voltages, which are used to turn the pixels on and off, because the LCD plasma tends to deteriorate whenever subjected to a DC voltage. It can be configured to toggle on every frame or to toggle every programmable number of VLINE signals.

Figure 15-4 shows the timing requirements for the LCD driver interface.

时序要求

应利用 VD[7：0]信号将视频数据从内存传送到 LCD 驱动器。VCLK 信号是将数据移入 LCD 驱动器中移位寄存器的时钟信号。一行数据被移入 LCD 驱动器中的移位寄存器后，便插入一个 VLINE 信号以显示此行（表明一行的结束）。

VM 信号则为显示器提供一个交流信号。LCD 用此信号使行和列电压的极性交替，这样可以使像素开或关，因为若用直流电压，LCD 中的等离子体会被破坏。VM 信号的可配置成每帧触发或在指定数量的 VLINE 信号后触发。

图 15-4 为 LCD 驱动器接口的时序要求。

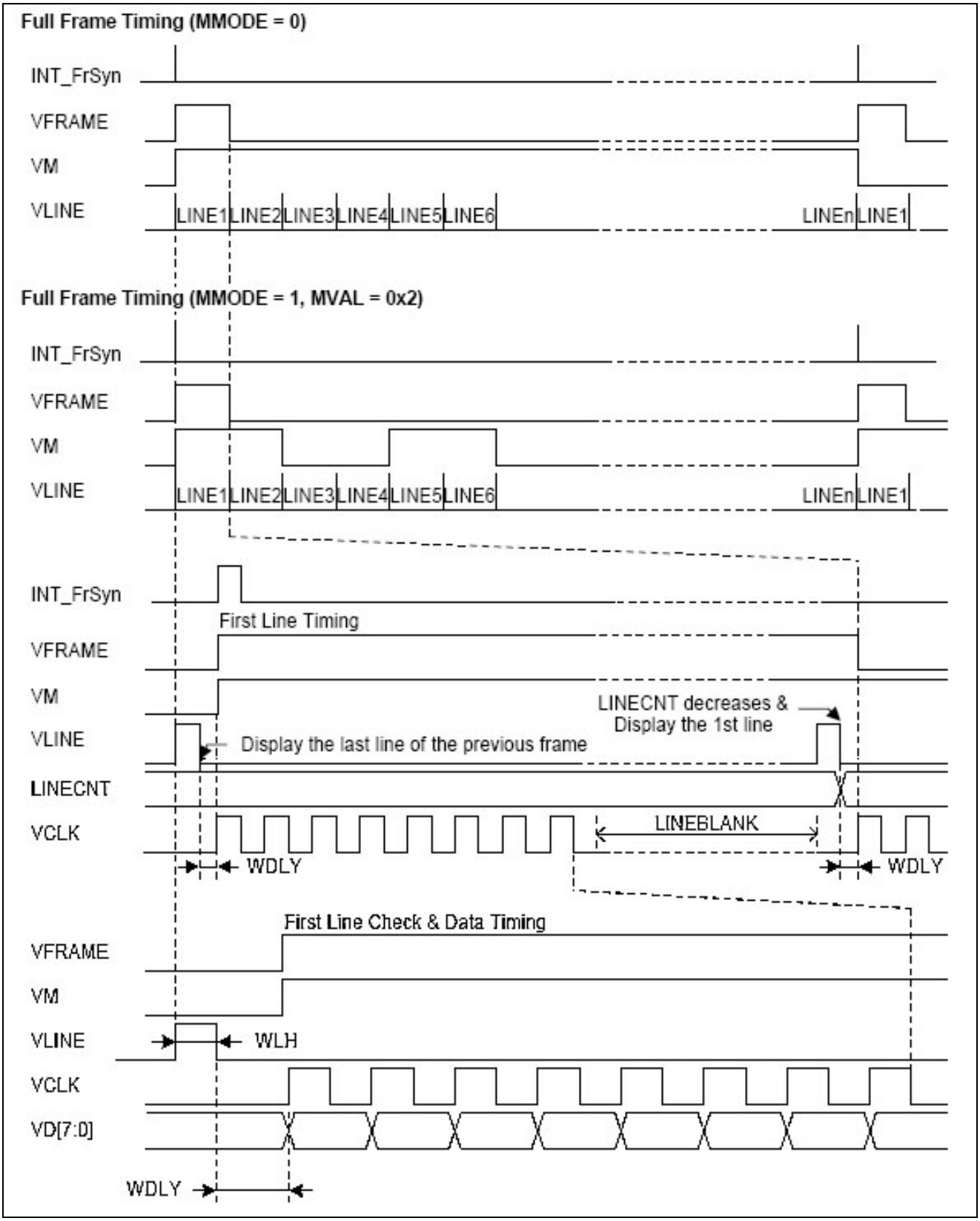


Figure 15-4. 8-bit Single Scan Display Type STN LCD Timing

图 15-4：8 位单扫描显示方式 STN 型 LCD 时序图

TFT LCD CONTROLLER OPERATION

TFT 型 LCD 控制器操作

The TIMEGEN generates the control signals for LCD driver, such as VSYNC, HSYNC, VCLK, VDEN, and LEND signal. These control signals are highly related with the configurations on the LCDCON1/2/3/4/5 registers in the REGBANK. Base on these programmable configurations on the LCD control registers in the REGBANK, the TIMEGEN can generate the programmable control signals suitable for the support of many different types of LCD drivers.

The VSYNC signal is asserted to cause the LCD's line pointer to start over at the top of the display.

TIMEGEN（脉冲发生器）生产适合 LCD 驱动器的各种控制信号，如 VSYNC, HSYNC, VCLK, VDEN,和 LEND 等信号。这些控制信号与寄存器组中的控制寄存器 LCDCON1/2/3/4/5 的配置密切相关。基于这些可编程 LCD 控制寄存器，肪冲发生器可以产生可编程的信号，可支持各种不同类型的 LCD 驱动器。

The VSYNC and HSYNC pulse generation depends on the configurations of both the HOZVAL field and the LINEVAL field in the LCDCON2/3 registers. The HOZVAL and LINEVAL can be determined by the size of the LCD panel according to the following equations:

HOZVAL = (Horizontal display size) -1

LINEVAL = (Vertical display size) -1

The rate of VCLK signal depends on the CLKVAL field in the LCDCON1 register. Table 15-3 defines the relationship of VCLK and CLKVAL. The minimum value of CLKVAL is 0.

VCLK(Hz) = HCLK/[(CLKVAL+1)x2]

VSYNC 和 HSYNC 脉问的产生取决于寄存器 LCDCON2/3 中 HOZVAL 与 LINEVAL 的配置值。HOZVAL 与 LINEVAL 的值与实际 LCD 屏和尺寸有关，公式如下：

HOZVAL = (水平显示尺寸) -1

LINEVAL = (垂直显示尺寸) -1

VCLK 的速率取决于寄存器 LCDCON1 中 CLKVAL 的值。表 15-3 定义了 VCLK 与 CLKVAL 之间的关系。CLKVAL 的最小值为 0。

VCLK(Hz) = HCLK/[(CLKVAL+1)x2]

The frame rate is VSYNC signal frequency. The frame rate is related with the field of VSYNC, VBPD, VFPD, LINEVAL, HSYNC, HBPD, HFPD, HOZVAL, and CLKVAL in LCDCON1 and LCDCON2/3/4 registers. Most LCD drivers need their own adequate frame rate. The frame rate is calculated as follows:

Frame Rate = 1/ [{ (VSPW+1) + (VBPD+1) + (LIINEVAL + 1) + (VFPD+1)}×{(HSPW+1) + (HBPD +1) + (HFPD+1) + (HOZVAL + 1) }×{ 2 ×(CLKVAL+1) / (HCLK) }]

帧频即为 VSYNC 信号的频率。帧频与控制寄存器 LCDCON1 及 LCDCON2/3/4 中的 VSYNC、VBPD、VFPD、LINEVAL、HSYNC、HBPD、HFPD、HOZVAL 和 CLKVAL 有关联。大多数 LCD 驱动器有它们适合的帧频。帧频可由下公式得出

Frame Rate = 1/[{(VSPW+1)+(VBPD+1)+(LIINEVAL+1)+(VFPD+1)}×{(HSPW+1)+(HBPD+1) +(HFPD+1)+(HOZVAL+1)}×{2×(CLKVAL+1)/(HCLK)}]

Table 15-3. Relation Between VCLK and CLKVAL (TFT, HCLK=60 MHz)

CLKVAL	60 MHz/X	VCLK
1	60 MHz/4	15.0 MHz
2	60 MHz/6	10.0 MHz
:	:	:
1023	60 MHz/2048	30.0 kHz

VIDEO OPERATION

The TFT LCD controller within the S3C2410X supports 1, 2, 4 or 8 bpp (bit per pixel) palettized color displays and 16 or 24 bpp non-palettized true-color displays.

256 Color Palette

The S3C2410X can support the 256 color palette for various selection of color mapping, providing flexible operation for users.

视频操作

S3C2410X 中 TFT LCD 控制器支持 1、2、4 或 8 位每像素带调色板显示和 16 或 24 位每像素无调色板真彩色显示。

256 色调色板

S3C2410X 支持多种颜色映射选择的 256 色调色板，使用户的操作更具弹性。

MEMORY DATA FORMAT (TFT)

内存中数据的格式（TFT）

This section includes some examples of each display mode.

这一部分包括每种显示模式的几个例子。

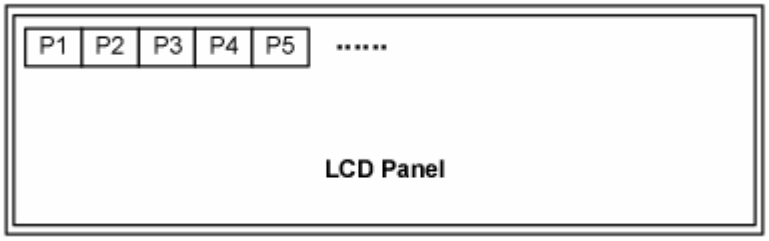
24BPP Display（24 位/像素显示）

(BSWP = 0, HWSWP = 0, BPP24BL = 0)

	D[31:24]	D[23:0]
000H	Dummy Bit	P1
004H	Dummy Bit	P2
008H	Dummy Bit	P3
...		

(BSWP = 0, HWSWP = 0, BPP24BL = 1)

	D[31:8]	D[7:0]
000H	P1	Dummy Bit
004H	P2	Dummy Bit
008H	P3	Dummy Bit
...		



VD Pin Descriptions at 24BPP（24 位/像素下 VD 引脚描述）

VD	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RED	7	6	5	4	3	2	1	0																
GREEN									7	6	5	4	3	2	1	0								
BLUE																	7	6	5	4	3	2	1	0

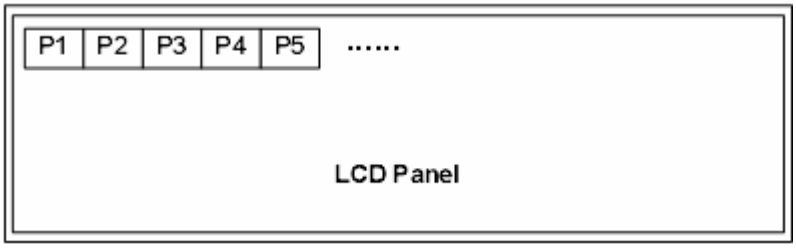
16BPP Display (16位/像素显示方式)

(BSWP = 0, HWSWP = 0)

	D[31:16]	D[15:0]
000H	P1	P2
004H	P3	P4
008H	P5	P6
...		

(BSWP = 0, HWSWP = 1)

	D[31:16]	D[15:0]
000H	P2	P1
004H	P4	P3
008H	P6	P5
...		



VD Pin Connections at 16BPP（16位/像素时VD引脚的连接）

(5:6:5)

VD	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RED	4	3	2	1	0	NC									NC							NC		
GREEN									5	4	3	2	1	0										
BLUE																	4	3	2	1	0			

(5:5:5:I)

VD	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RED	4	3	2	1	0	I	NC								NC								NC	
GREEN									4	3	2	1	0	I										
BLUE																	4	3	2	1	0	I		

NOTE: The unused VD pins can be used as GPIO.

注意：未使用的VD引脚可用作GPIO

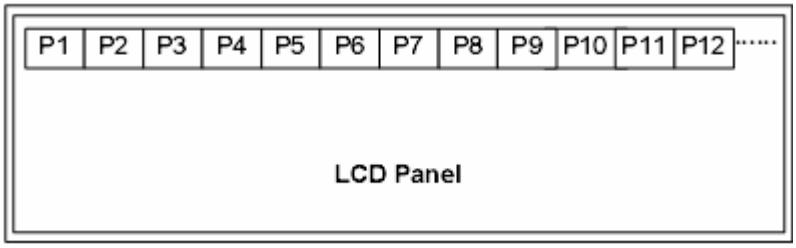
8BPP Display（8位/像素显示方式）

(BSWP = 0, HWSWP = 0)

	D[31:24]	D[23:16]	D[15:8]	D[7:0]
000H	P1	P2	P3	P4
004H	P5	P6	P7	P8
008H	P9	P10	P11	P12
...				

(BSWP = 1, HWSWP = 0)

	D[31:24]	D[23:16]	D[15:8]	D[7:0]
000H	P4	P3	P2	P1
004H	P8	P7	P6	P5
008H	P12	P11	P10	P9
...				



4BPP Display（4位/像素显示方式）

(BSWP = 0, HWSWP = 0)

	D[31:28]	D[27:24]	D[23:20]	D[19:16]	D[15:12]	D[11:8]	D[7:4]	D[3:0]
000H	P1	P2	P3	P4	P5	P6	P7	P8
004H	P9	P10	P11	P12	P13	P14	P15	P16
008H	P17	P18	P19	P20	P21	P22	P23	P24
...								

(BSWP = 1, HWSWP = 0)

	D[31:28]	D[27:24]	D[23:20]	D[19:16]	D[15:12]	D[11:8]	D[7:4]	D[3:0]
000H	P7	P8	P5	P6	P3	P4	P1	P2
004H	P15	P16	P13	P14	P11	P12	P9	P10
008H	P23	P24	P21	P22	P19	P20	P17	P18
...								

2BPP Display（2位/像素显示方式）

(BSWP = 0, HWSWP = 0)

D	[31:30]	[29:28]	[27:26]	[25:24]	[23:22]	[21:20]	[19:18]	[17:16]
000H	P1	P2	P3	P4	P5	P6	P7	P8
004H	P17	P18	P19	P20	P21	P22	P23	P24
008H	P33	P34	P35	P36	P37	P38	P39	P40
...								

D	[15:14]	[13:12]	[11:10]	[9:8]	[7:6]	[5:4]	[3:2]	[1:0]
000H	P9	P10	P11	P12	P13	P14	P15	P16
004H	P25	P26	P27	P28	P29	P30	P31	P32
008H	P41	P42	P43	P44	P45	P46	P47	P48
...								

256 PALETTE USAGE (TFT)

Palette Configuration and Format Control

The S3C2410X provides 256 color palette for TFT LCD Control.

The user can select 256 colors from the 64K colors in these two formats.

The 256 color palette consists of the 256 (depth)×16-bit SPSRAM. The palette supports 5:6:5 (R:G:B) format and 5:5:5:1(R:G:B:I) format.

When the user uses 5:5:5:1 format, the intensity data(I) is used as a common LSB bit of each RGB data. So, 5:5:5:1 format is the same as R(5+I):G(5+I):B(5+I) format.

In 5:5:5:1 format, for example, the user can write the palette as in Table 15-5 and then connect VD pin to TFT LCD panel(R(5+I)=VD[23:19]+VD[18], VD[10] or VD[2], G(5+I)=VD[15:11]+ VD[18], VD[10] or VD[2], B(5+I)=VD[7:3]+ VD[18], VD[10] or VD[2].), and set FRM 565 of LCDCON5 register to 0.

调色板的配置和格式控制。

S3C2410X 为 TFT 型 LCD 控制提供了 256 色调色板。

在这两种格式中用户可以从 64K 种颜色选择 256 种颜色显示。

256 色调色板由 256(深度)×16 位 SPSRAM 组成,这种调色板可支持 5:6:5(R:G:B)和 5:5:5:1(R:G:B:I)两种格式。

当用户使用 5:5:5:1 格式时,亮度数据(I)可用作每个 GRB 数据的共同 LSB(最低有效位),即:5:5:5:1 格式等同于 R(5+I):G(5+I):B(5+I)格式。

使用 5:5:5:1 格式时,例如,用户可如表 15-5 那样配置调色板,然后将引脚 VD 接到 TFTLCD 屏(其中 R(5+I)=VD[23:19]+VD[18],VD[10] 或 VD[2],G(5+I)=VD[15:11]+VD[18],VD[10] 或 VD[2],B(5+I)=VD[7:3]+ VD[18], VD[10]或 VD[2]),将寄存器 LCDCON5 中的 FRM565 设置成 0。

Table 15-4. 5:6:5 Format

INDEX\Bit Pos.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
00H	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0	0X4D000400 (note1)
01H	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0	0X4D000404
.....																	.....
FFH	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0	0X4D0007FC
Number of VD	23	22	21	20	19	15	14	13	12	11	10	7	6	5	4	3	

Table 15-5. 5:5:5:1 Format

INDEX\Bit Pos.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
00H	R4	R3	R2	R1	R0	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0	I	0X4D000400
01H	R4	R3	R2	R1	R0	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0	I	0X4D000404
.....																	.....
FFH	R4	R3	R2	R1	R0	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0	I	0X4D0007FC
Number of VD	23	22	21	20	19	15	14	13	12	11	7	6	5	4	3	2)	

NOTES:

1. 0x4D000400 is Palette start address.
2. VD18, VD10 and VD2 have the same output value, I.
3. DATA[31:16] is invalid.

注意:

1、0x4D000400 是调色板起始地址。

2、VD18、VD10 和 VD2 的输出值是一样的,即 I。

3、DATA[31:16]是未用的。

Palette Read/Write

When the user performs Read/Write operation on the palette, HSTATUS and VSTATUS of LCDCON5 register must be checked, for Read/Write operation is prohibited during the ACTIVE status of

HSTATUS and VSTATUS.

调色板读写

当用户在调色板上执行读写操作时，需检查一下寄存器 LCDCON5 中的 HSTATUS 和 VSTATUS，因为在 HSTATUS 和 VSTATUS 状态为 ACTIVE 期间，读写操作是禁止执行的。

Temporary Palette Configuration

The S3C2410X allows the user to fill a frame with one color without complex modification to fill the one color to the frame buffer or palette. The one colored frame can be displayed by the writing a value of the color which is displayed on LCD panel to TPALVAL of TPAL register and enable TPALEN.

调色板的临时配置

S3C2410X 充许用户在没有大的修改的情况下对一帧填入一种颜色，这样可以将帧缓冲或调色板填入一种颜色。要显示同种颜色的一帧，可将要显示的颜色的值写入寄存器 TPAL 中的 TPALVAL 并且将 TPALEN 置 1。

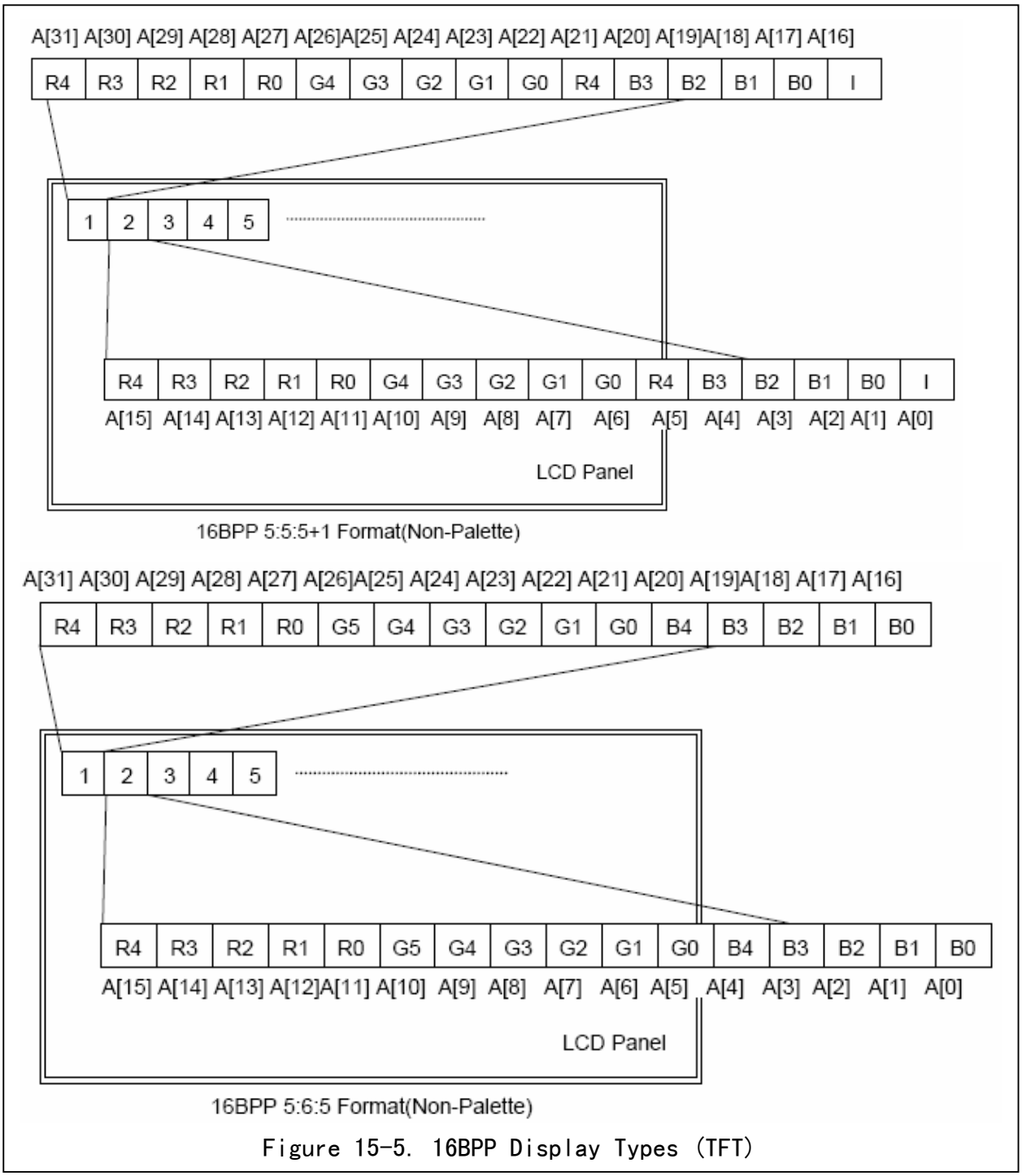


Figure 15-5. 16BPP Display Types (TFT)

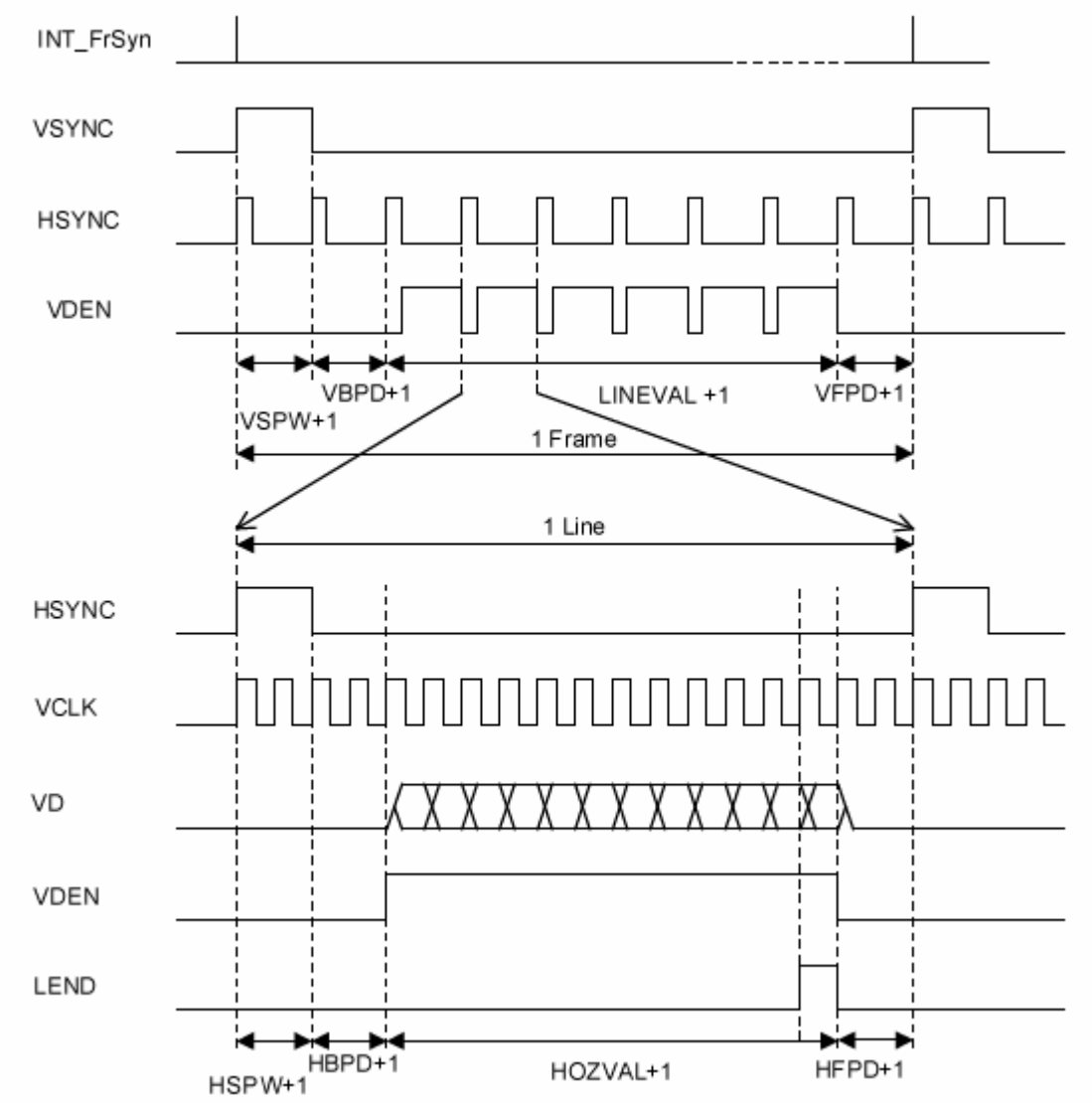


Figure 15-6. TFT LCD Timing Example

SAMSUNG TFT LCD PANEL (3.5 PORTRAIT / 256K COLOR /REFLECTIVE A-SI TFT LCD)

The S3C2410X supports SEC TFT LCD panel (SAMSUNG 3.5 Portrait / 256K Color /Reflective a-Si TFT LCD).

LTS350Q1-PD1: TFT LCD panel with touch panel and front light unit
LTS350Q1-PD2: TFT LCD panel only

The S3C2410X provides timing signals as follows to use LTS350Q1-PD1 and PD2:

STH	:Horizontal Start Pulse
TP	:Source Driver Data Load Pulse
INV	:Digital Data Inversion
LCD_HCLK	:Horizontal Sampling Clock
CPV	:Vertical Shift Clock
STV	:Vertical Start Pulse
OE	:Gate On Enable
REV	:Inversion Signal
REVB	:Inversion Signal

So, LTS350Q1-PD1 and PD2 can be connected with the S3C2410X without using the additional timing control logic.
But the user should additionally apply Vcom generator circuit, various voltages, INV signal and Gray scale voltage generator circuit, which is recommended by PRODUCT INFORMATION (SPEC) of LTS350Q1-PD1 and PD2.
Detailed timing diagram is also described in PRODUCT INFORMATION (SPEC) of LTS350Q1-PD1 and PD2.

Refer to the documentation (PRODUCT INFORMATION of LTS350Q1-PD1 and PD2), which is prepared by AMLCD Technical Customer Center of Samsung Electronics Co., LTD.

Caution:

The S3C2410X has HCLK, working as the clock of AHB bus.
Accidentally, SEC TFT LCD panel (LTS350Q1-PD1 and PD2) has Horizontal Sampling Clock (HCLK). These two HCLKs may cause a confusion. So, note that HCLK of the S3C2410X is HCLK and other HCLK of the LTS350 is LCD_HCLK.

Check that the HCLK of SEC TFT LCD panel (LTS350Q1-PD1 and PD2) is changed to LCD_HCLK.

VIRTUAL DISPLAY (TFT/STN)]

The S3C2410X supports hardware horizontal or vertical scrolling. If the screen is scrolled, the fields of LCDBASEU and LCDBASEL in LCDSADDR1/2 registers need to be changed (see Figure 15-8), except the values of PAGEWIDTH and OFFSIZE.
The video buffer in which the image is stored should be larger than the LCD panel screen in size.

虚拟显示（TFT/STN）

S3C2410X 支持硬件方式的水平和垂直滚屏。要实现滚屏，可修改 LCDSADDR1 和 LCDSADDR2 寄存器中的 LCDBASEU 和 LCDBASEL 的值（如图 15-8）。但不是通过修改 PAGEWIDTH 和 OFFSIZE 来实现。

显示缓冲区中的图像在尺寸上应比 LCD 显示屏大些。

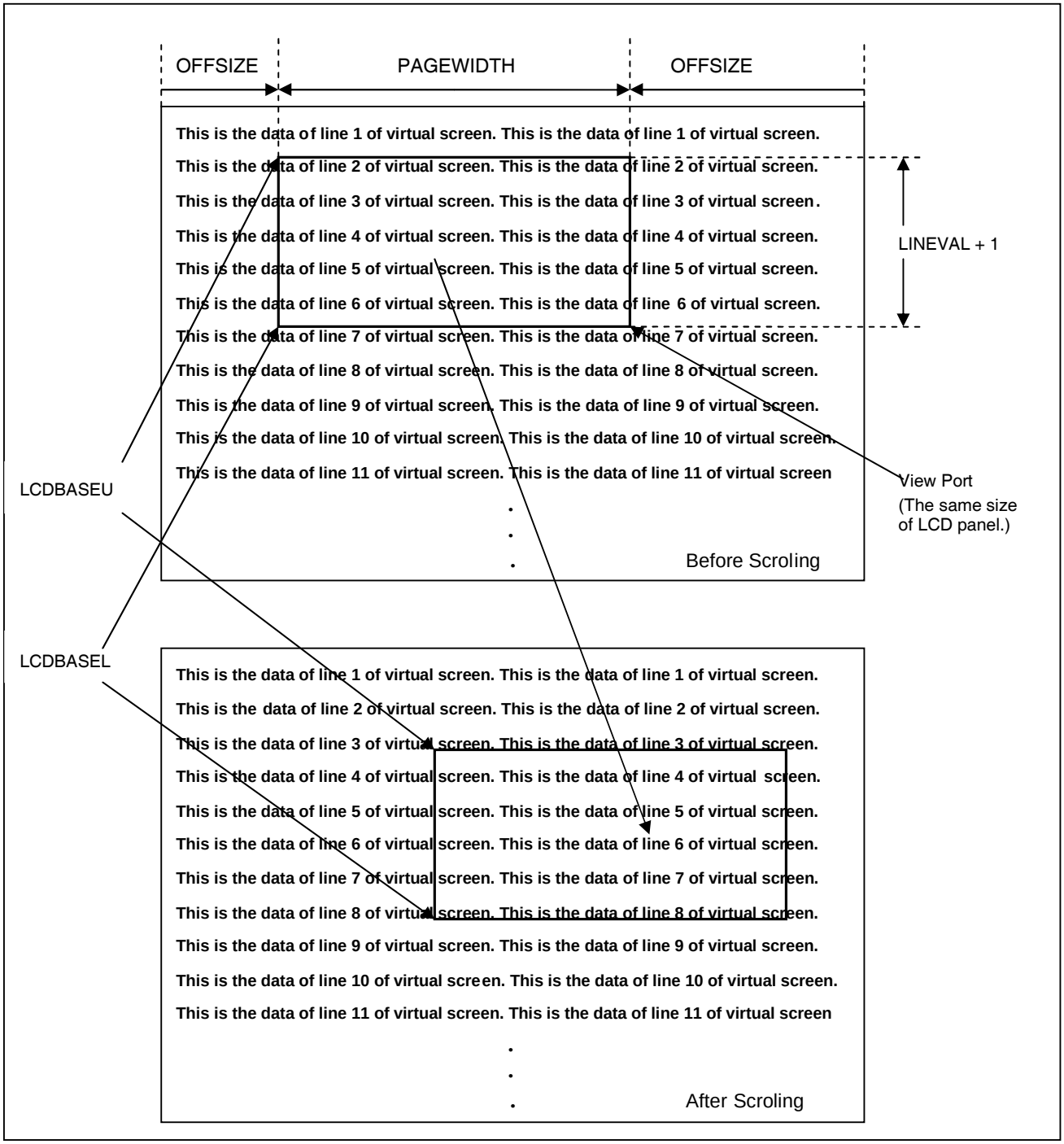


Figure 15-7. Example of Scrolling in Virtual Display (Single Scan)
图 15-7：虚拟显示滚屏（单扫描）示例

LCD POWER ENABLE (STN/TFT)

The S3C2410X provides Power enable (PWREN) function. When PWREN is set to make PWREN signal enabled, the output value of LCD_PWREN pin is controlled by ENVID. In other words, If LCD_PWREN pin is connected to the power on/off control pin of the LCD panel, the power of LCD panel is controlled by the setting of ENVID automatically.

The S3C2410X also supports INVPWREN bit to invert polarity of the PWREN signal.

This function is available only when LCD panel has its own power on/off control port and when port is connected to LCD_PWREN pin.

LCD 的电源控制(STN/TFT)

S3C2410X 有电源控制（PWREN）功能。启用电源控制时，引脚 LCD_PWREN 的输出值是由 ENVID 控制的。换言之，当引脚 LCD_PWREN 连接至 LCD 屏的电源开头控制端后，LCD 屏的电源就自动由 ENVID 的设置确定。

S3C2410X 亦有极性反转位（INVPWREN），可以 PWREN 信号的极性反转。

此功能只有当 LCD 屏有电源控制端口且被正确连接至 LCD_PWREN 引脚时方为有效。

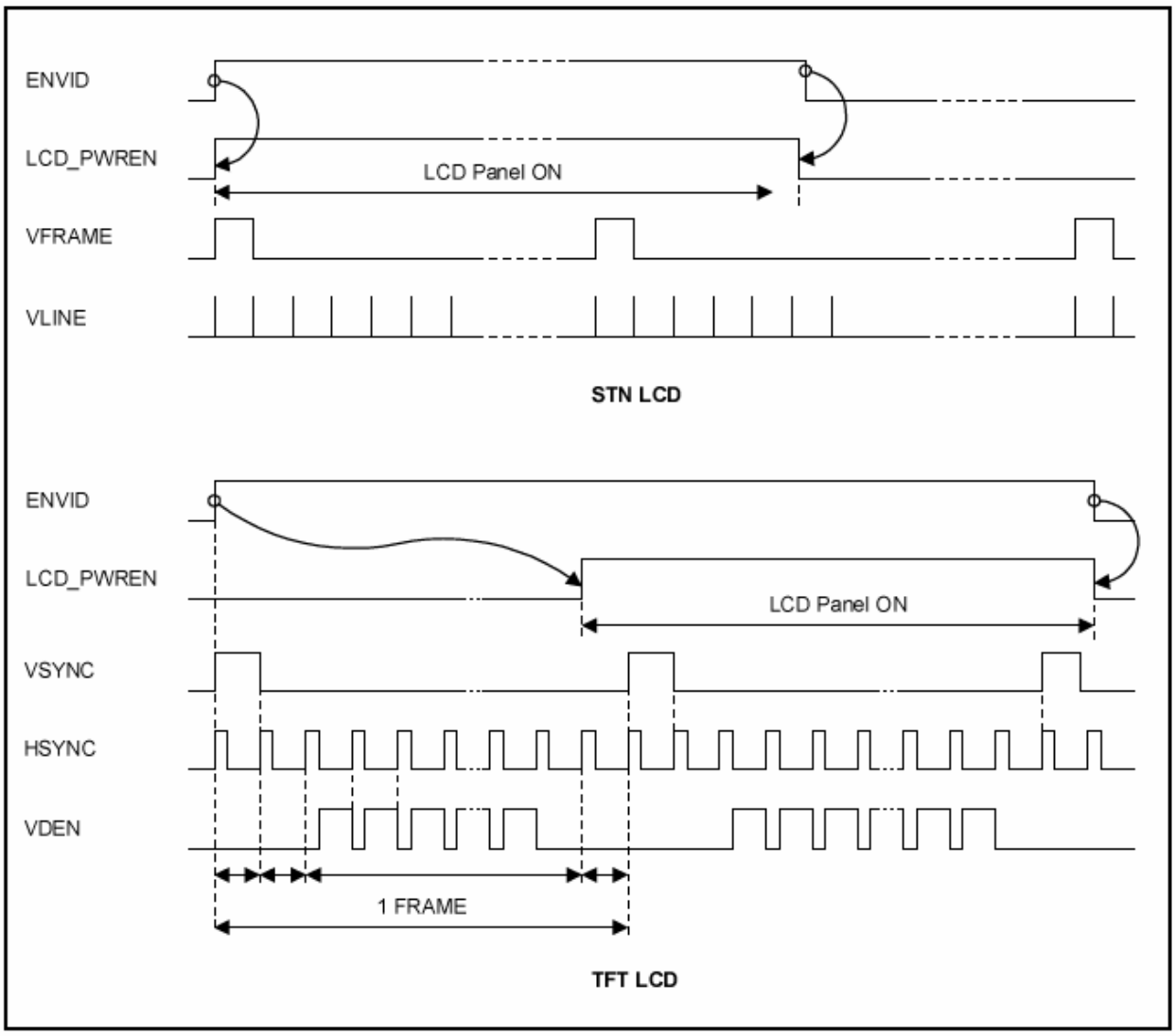


Figure 15-8. Example of PWREN Function (PWREN = 1, INVPWREN = 0)

LCD CONTROLLER SPECIAL REGISTERS

LCD Control 1 Register

Register	Address	R/W	Description	Reset Value
LCDCON1	0X4D000000	R/W	LCD control 1 register	0x00000000

LCDCON1	Bit	Description	Initial State
LINECNT (read only)	[27:18]	Provide the status of the line counter. Down count from LINEVAL to 0	0000000000
CLKVAL	[17:8]	Determine the rates of VCLK and CLKVAL[9:0]. **STN**: VCLK = HCLK / (CLKVAL×2) (CLKVAL≧2) **TFT**: VCLK = HCLK / [(CLKVAL+1) × 2] (CLKVAL≧0)	0000000000
MMODE	[7]	Determine the toggle rate of the VM. 0 = Each Frame, 1 = The rate defined by the MVAL	0
PNRMODE	[6:5]	Select the display mode. 00 = 4-bit dual scan display mode (STN) 01 = 4-bit single scan display mode (STN) 10 = 8-bit single scan display mode (STN) 11 = TFT LCD panel	00
BPPMODE	[4:1]	Select the BPP (Bits Per Pixel) mode. 0000 = 1 bpp for STN, Monochrome mode 0001 = 2 bpp for STN, 4-level gray mode 0010 = 4 bpp for STN, 16-level gray mode 0011 = 8 bpp for STN, color mode 0100 = 12 bpp for STN, color mode 1000 = 1 bpp for TFT 1001 = 2 bpp for TFT 1010 = 4 bpp for TFT 1011 = 8 bpp for TFT 1100 = 16 bpp for TFT 1101 = 24 bpp for TFT	0000
ENVID	[0]	LCD video output and the logic enable/disable. 0 = Disable the video output and the LCD control signal. 1 = Enable the video output and the LCD control signal.	0

LCD 控制器的专用寄存器

LCD 控制寄存器 1

寄存器	地址	R/W	描述	复位值
LCDCON1	0X4D000000	R/W	LCD 控制寄存器 1	0x00000000

LCDCON1	Bit	描述	初始值
LINECNT (只读)	[27:18]	行计数器状态位，值由 LINEVAL 递减至 0	0000000000
CLKVAL	[17:8]	Determine the rates of VCLK and CLKVAL[9:0]. **STN**: VCLK = HCLK / (CLKVAL×2) (CLKVAL≧2) **TFT**: VCLK = HCLK / [(CLKVAL+1) × 2] (CLKVAL≧0)	0000000000
MMODE	[7]	决定VM信号的触发速率。 0 = 每帧触发, 1 = 触发速率由MVAL决定	0
PNRMODE	[6:5]	显示模式选择位 00 = 4位双扫描显示模式(STN) 01 = 4位单扫描显示模式(STN) 10 = 8位单扫描显示模式(STN) 11 = TFT型LCD显示	00
BPPMODE	[4:1]	单个像素的位数选择 0000 = STN型1位/像素, 单色模式 0001 = STN型2位/像素, 4级灰度模式 0010 = STN型4位/像素16级灰度模式 0011 = STN型8位/像素, 彩色模式 0100 = STN型12位/像素, 彩色模式 1000 = TFT型1位/像素 1001 = TFT型2位/像素 1010 = TFT型4位/像素 1011 = TFT型8位/像素 1100 = TFT型16位/像素 1101 = TFT型24位/像素	0000
ENVID	[0]	LCD视频输出和逻辑信号使能位 0 = 视频输出和控制信号无效 1 =视频输出和控制信号有效	0

LCD Control 2 Register

Register	Address	R/W	Description	Reset Value
LCDCON2	0X4D000004	R/W	LCD control 2 register	0x00000000

LCDCON2	Bit	Description	Initial State
VBPD	[31:24]	**TFT**: Vertical back porch is the number of inactive lines at the start of a frame, after vertical synchronization period. **STN**: These bits should be set to zero on STN LCD.	0x00
LINEVAL	[23:14]	**TFT/STN**: These bits determine the vertical size of LCD panel.	0000000000
VFPD	[13:6]	**TFT**: Vertical front porch is the number of inactive lines at the end of a frame, before vertical synchronization period. **STN**: These bits should be set to zero on STN LCD.	00000000
VSPW	[5:0]	**TFT**: Vertical sync pulse width determines the VSYNC pulse's high level width by counting the number of inactive lines. **STN**: These bits should be set to zero on STN LCD.	000000

控制寄存器2

寄存器	地址	R/W	描述	复位值
LCDCON2	0X4D000004	R/W	LCD 控制寄存器 2	0x00000000

LCDCON2	位	描述	初始状态
VBPD	[31:24]	**TFT**: 垂直后沿（VBPD）指在一帧开始时，垂直同步时期之后非活动行的数目。 **STN**: 使用STN型LCD时此位应为0	0x00
LINEVAL	[23:14]	**TFT/STN**: 这些位决定 LCD 屏的垂直尺寸	0000000000
VFPD	[13:6]	**TFT**: 垂直后沿指在一帧结束时，垂直同步时期后非活动行的数目。 **STN**: 使用STN型LCD时此位应为0	00000000
VSPW	[5:0]	**TFT**: 通过对非活动行的计数，垂直同步脉冲宽度决定着VSYNC脉冲高电平宽度。 **STN**: 使用STN型LCD时此位应为0	000000

LCD Control 3 Register

Register	Address	R/W	Description	Reset Value
LCDCON3	0X4D000008	R/W	LCD control 3 register	0x00000000

LCDCON3	Bit	描述	Initial state
HBPD (TFT)	[25:19]	**TFT**: Horizontal back porch is the number of VCLK periods betweenthe falling edge of HSYNC and the start of active data.	0000000
WDLY (STN)		**STN**: WDLY[1:0] bits determine the delay between VLINE and VCLK by counting the number of the HCLK. WDLY[7:2] are reserved. 00 = 16 HCLK, 01 = 32 HCLK, 10 = 48 HCLK, 11 = 64 HCLK	
HOZVAL	[18:8]	**TFT/STN**: These bits determine the horizontal size of LCD panel. HOZVAL has to be determined to meet the condition that total bytes of 1 line are 4n bytes. If the x size of LCD is 120 dot in mono mode, x=120 cannot be supported because 1 line consists of 15 bytes. Instead, x=128 in mono mode can be supported because 1 line is composed of 16 bytes (2n). LCD panel driver will discard the additional 8 dot.	00000000000
HFPD (TFT)	[7:0]	**TFT**: Horizontal front porch is the number of VCLK periods between the end of active data and the rising edge of HSYNC.	0X00
LINEBLANK (STN)		**STN**: These bits indicate the blank time in one horizontal line duration time. These bits adjust the rate of the VLINE finely. The unit of LINEBLANK is HCLK X 8. Ex) If the value of LINEBLANK is 10, the blank time is inserted to VCLK during 80 HCLK.	

控制寄存器3

寄存器	地址	R/W	描述	复位值
LCDCON3	0X4D000008	R/W	LCD 控制寄存器 3	0x00000000

LCDCON3	Bit	描述	初始状态
HBPD (TFT)	[25:19]	**TFT**: 水平后沿（HBPD）为HSYNC下降沿后与有效数据之前VCLK的周期数目。	0000000
WDLY (STN)		**STN**: WDLY[1:0]位通过对HCLK的计数决定VLINE与VCLK之间的延迟。WDLY[7:2]为保留位。 00 = 16 HCLK, 01 = 32 HCLK, 10 = 48 HCLK, 11 = 64 HCLK	
HOZVAL	[18:8]	**TFT/STN**:这些位决定着LCD屏水平尺寸，HOZVAL必须被指定以满足一行有4n个字节的条件。如单色模式下LCD一行有120个点，但120点是不被支持的，因为1行要由15个字节组成。而单色模式下一行128个点是可以支持的，因为一行有16(2n)个字节组成。LCD屏将丢弃多余的8个点。	00000000000
HFPD (TFT)	[7:0]	**TFT**: 水平前沿（HFPD）为有效数据之后与HSYNC上升沿前VCLK的周期数目。	0X00
LINEBLANK (STN)		**STN**: 这些位确定行扫描的返回时间.这些位可微调VLINE的速率。LINEBLANK的最小数为HCLK*8。如：LINEBLANK=10，返回时间在80个HCLK期间插入VCLK。	

LCD Control 4 Register

Register	Address	R/W	Description	Reset Value
LCDCON4	0X4D00000C	R/W	LCD control 4 register	0x00000000

LCDCON4	Bit	Description	Initial state
MVAL	[15:8]	**STN**: These bit define the rate at which the VM signal will toggle if the MMODE bit is set to logic '1'.	0X00
HSPW(TFT)	[7:0]	**TFT**: Horizontal sync pulse width determines the HSYNC pulse's high level width by counting the number of the VCL K.	0X00
WLH(STN)		**STN**: WLH[1:0] bits determine the VLINE pulse's high level width by counting the number of the HCLK. WLH[7:2] are reserved. 00 = 16 HCLK, 01 = 32 HCLK, 10 = 48 HCLK, 11 = 64 HCLK	

LCD 控制寄存器 4

Register	Address	R/W	Description	Reset Value
LCDCON4	0X4D00000C	R/W	LCD 控制寄存器 4	0x00000000

LCDCON4	Bit	Description	Initial state
MVAL	[15:8]	**STN**: 如果 MMODE=1,这两位定义 VM 信号以什么速度变化	0X00
HSPW(TFT)	[7:0]	**TFT**: 通过对VCLK的计数水平同步脉冲宽度决定着HSYNC脉高电平脉冲的宽度。	0X00
WLH(STN)		**STN**: 通过过HCLK的计数，WLH[1:0] 位决定着VLINE脉冲的高电平宽度。而WLH[7:2]作为保留位。 00 = 16 HCLK, 01 = 32 HCLK, 10 = 48 HCLK, 11 = 64 HCLK	

LCD Control 5 Register

Register	Address	R/W	Description	Reset Value
LCDCON5	0X4D000010	R/W	LCD control 5 register	0x00000000

LCDCON5	Bit	Description	Initial state
Reserved	[31:17]	This bit is reserved and the value should be '0'	0
VSTATUS	[16:15]	TFT: Vertical Status (read only). 00 = VSYNC 01 = BACK Porch 10 = ACTIVE 11 = FRONT Porch	00
HSTATUS	[14:13]	TFT: Horizontal Status (read only). 00 = HSYNC 01 = BACK Porch 10 = ACTIVE 11 = FRONT Porch	00
BPP24BL	[12]	T FT: This bit determines the order of 24 bpp video memory. 0 = LSB valid 1 = MSB Valid	0
FRM565	[11]	TFT: This bit selects the format of 16 bpp output video data. 0 = 5:5:5:1 Format 1 = 5:6:5 Format	0
INVVCLK	[10]	STN/TFT: This bit controls the polarity of the VCLK active edge. 0 = The video data is fetched at VCLK falling edge 1 = The video data is fetched at VCLK rising edge	0
INVVLINE	[9]	STN/TFT: This bit indicates the VLINE/HSYNC pulse polarity. 0 = Normal 1 = Inverted	0
INVVFRAME	[8]	STN/TFT: This bit indicates the VFRAME/VSYNC pulse polarity. 0 = Normal 1 = Inverted	0
INVVD	[7]	STN/TFT: This bit indicates the VD (video data) pulse polarity. 0 = Normal1 = VD is inverted.	0
INVVDEN	[6]	TFT: This bit indicates the VDEN signal polarity. 0 = Normal 1 = Inverted	0
INVPWREN	[5]	STN/TFT: This bit indicates the PWREN signal polarity. 0 = Normal 1 = Inverted	0
INVLEND	[4]	TFT: This bit indicates the LEND signal polarity. 0 = Normal 1 = Inverted	0
PWREN	[3]	STN/TFT: LCD_PWREN output signal enable/disable. 0 = Disable PWREN signal 1 = Enable PWREN signal	0
ENLEND	[2]	TFT: LEND output signal enable/disable. 0 = Disable LEND signal 1 = Enable LEND signal	0
BSWP	[1]	STN/TFT: Byte swap control bit. 0 = Swap Disable 1 = Swap Enable	0
HWSWP	[0]	STN/TFT: Half-Word swap control bit. 0 = Swap Disable 1 = Swap Enable	0

LCD 控制寄存器 5

Register	Address	R/W	Description	Reset Value
LCDCON5	0X4D000010	R/W	LCD 控制寄存器 5	0x00000000

LCDCON5	Bit	Description	Initial state
保留	[31:17]	这些位是保留位，值为 0。	0
VSTATUS	[16:15]	TFT: 垂直扫描状态 (只读). 00 = VSYNC 01 = BACK Porch 10 = ACTIVE 11 = FRONT Porch	00
HSTATUS	[14:13]	TFT: 水平扫描状态 (只读). 00 = HSYNC 01 = BACK Porch 10 = ACTIVE 11 = FRONT Porch	00
BPP24BL	[12]	TFT: 这些位确定中 24bpp 显示时显存中数据的格式。 0 = LSB 有效 1 = MSB 有效	0
FRM565	[11]	TFT: 这些位确定 16bpp 显示时输出数据的格式。 0 = 5:5:5:1 格式 1 = 5:6:5 格式	0
INVVCLK	[10]	STN/TFT: 这一位决定 VCLK 的有效极性。 0 = VCLK 下降沿时取数据。 1 = VCLK 上升沿时取数据。	0
INVVLINE	[9]	STN/TFT:此位指明 VLINE/HSYNC 脉冲的极性。 0 = 正常 1 = 反转	0
INVVFRAME	[8]	STN/TFT:此位指明 VFRAME/VSYNC 脉冲的极性。 0 = 正常 1 = 反转	0
INVVD	[7]	STN/TFT:此位指明 VD (视频数据)脉冲的极性。 0 = 正常 1 = VD 反转	0
INVVDEN	[6]	TFT:此位指明 VDEN 信号的极性。 0 = 正常 1 = 反转	0
INVPWREN	[5]	STN/TFT:此位指明 PWREN 信号的极性。 0 = 正常 1 = VD 反转	0
INVLEND	[4]	TFT:此位指明 LEND 信号的极性。 0 = 正常 1 = VD 反转	0
PWREN	[3]	STN/TFT: LCD_PWREN 输出信号使能位。 0 = PWREN 信号无效 1 = PWREN 信号有效	0
ENLEND	[2]	TFT: LEND 输出信号使能位。 0 = LEND 信号无效 1 = LEND 信号有效	0
BSWP	[1]	STN/TFT: 字节交换控制位。 0 = 不可交换 1 = 可以交换	0
HWSWP	[0]	STN/TFT: 半字交换控制位。 0 = 不可交换 1 = 可以交换	0

FRAME BUFFER START ADDRESS 1 REGISTER

Register	Address	R/W	Description	Reset Value
LCDSADDR1	0X4D000014	R/W	**STN/TFT**: Frame buffer start address 1 register.	0x00000000

LCDSADDR1	Bit	Description	Initial State
LCDBANK	[29:21]	These bits indicate A[30:22] of the bank location for the video buffer in the system memory. LCDBANK value cannot be changed even when moving the view port. LCD frame buffer should be within aligned 4MB region, which ensures that LCDBANK value will not be changed when moving the view port. So, care should be taken to use the malloc() function.	0x00
LCDBASEU	[20:0]	For dual-scan LCD: These bits indicate A[21:1] of the start address of the upper address counter, which is for the upper frame memory of dual scan LCD or the frame memory of single scan LCD. For single-scan LCD: These bits indicate A[21:1] of the start address of the LCD frame buffer.	0x000000

帧缓冲起始地址寄存器1

Register	Address	R/W	Description	Reset Value
LCDSADDR1	0X4D000014	R/W	**STN/TFT**: 帧缓冲起始地址寄存器1	0x00000000

LCDSADDR1	Bit	Description	Initial State
LCDBANK	[29:21]	这些位指明在系统内存中视频缓冲区的位置A[30:22]。LCDBANK的值是不可被改变的，移动观察窗口时也是一样。LCD帧缓冲应保证在4MB的连续区域内，以确保在移动观察窗口时LCDBANK的值不被改变。所以，在使用函数malloc()时务必要小心。	0x00
LCDBASEU	[20:0]	**对双扫描LCD：**这些位指示帧缓冲区或在双扫描LCD时的上帧缓冲区的开始地址 A[21:1] **对单扫描LCD：**这些位指示帧缓冲区的开始地址 A[21:1]	0x000000

FRAME Buffer Start Address 2 Register

Register	Address	R/W	Description	Reset Value
LCDSADDR2	0X4D000018	R/W	**STN/TFT**: Frame buffer start address 2 register	0x00000000

LCDSADDR2	Bit	Description	Initial State
LCDBASEL	[20:0]	For dual-scan LCD: These bits indicate A[21:1] of the start address of the lower address counter, which is used for the lower frame memory of dual scan LCD. For single scan LCD: These bits indicate A[21:1] of the end address of the LCD frame buffer. LCDBASEL = ((the fame end address) >>1) + 1 = LCDBASEU + (PAGEWIDTH+OFFSIZE)x(LINEVAL+1)	0x0000

帧缓冲起始地址寄存器2

Register	Address	R/W	Description	Reset Value
LCDSADDR2	0X4D000018	R/W	**STN/TFT**：帧缓冲起始地址寄存器2	0x00000000

LCDSADDR2	Bit	Description	Initial State
LCDBASEL	[20:0]	**对于双扫描LCD**：这些位指示在使用双扫描LCD时的下帧存储区的开始地址 A[21:1]。 **对于单扫描LCD**：这些位指示帧存储区的末地址 A[21:1] LCDBASEL = ((the fame end address) >>1) + 1 = LCDBASEU +(PAGEWIDTH+OFFSIZE)x(LINEVAL+1)	0x0000

NOTE: Users can change the LCDBASEU and LCDBASEL values for scrolling while the LCD controller is turned on. But, users must not change the value of the LCDBASEU and LCDBASEL registers at the end of FRAME by referring to the LINECNT field in LCDCON1 register, for the LCD FIFO fetches the next frame data prior to the change in the frame. So, if you change the frame, the pre-fetched FIFO data will be obsolete and LCD controller will display an incorrect screen. To check the LINECNT, interrupts should be masked. If any interrupt is executed just after reading **LINECNT**,
the read LINECNT value may be obsolete because of the execution time of Interrupt Service Routine (ISR).

注意：当 LCD 控制器起用时，用户可通过改变 LCDBASEU 和 LCDBASEL 的值实现滚屏。但是，在一帧结束时，LCDBASEU 和 LCDBASEL 的值务必不能改变，可参考 LCDCON1 寄存器中的 LINECNT 域，因为 LCD 的 FIFO 是在换帧前取数据的。所以，若这时你要换帧，预取的 FIFO 数据将被丢弃，LCD 屏的显示也会出现错误。检查 LINECNT 时，需先屏蔽所有中断。否则，由于中断服务程序的执行时间，读取的 LINECNT 的值也会被丢弃。

FRAME Buffer Start Address 3 Register

Register	Address	R/W	Description	Reset Value
LCDSADDR3	0X4D00001C	R/W	**STN/TFT**: Virtual screen address set	0x00000000

LCDSADDR3	Bit	Description	Initial State
OFFSIZE	[21:11]	Virtual screen offset size (the number of half words). This value defines the difference between the address of the last half word displayed on the previous LCD line and the address of the first half word to be displayed in the new LCD line.	00000000000
PAGEWIDTH	[10:0]	Virtual screen page width (the number of half words). This value defines the width of the view port in the frame.	000000000

帧缓冲起始地址寄存器3

Register	Address	R/W	Description	Reset Value
LCDSADDR3	0X4D00001C	R/W	**STN/TFT**: 虚拟屏地址设置	0x00000000

LCDSADDR3	Bit	Description	Initial State
OFFSIZE	[21:11]	Virtual screen offset size (the number of half words). This value defines the difference between the address of the last half word displayed on the previous LCD line and the address of the first half word to be displayed in the new LCD line.	00000000000
PAGEWIDTH	[10:0]	Virtual screen page width (the number of half words). This value defines the width of the view port in the frame.	000000000

NOTE: The values of PAGEWIDTH and OFFSIZE must be changed when ENVID bit is 0.

```
Example 1. LCD panel = 320*240, 16gray, single scan
        Frame start address = 0x0c500000
        Offset dot number = 2048 dots ( 512 half words )

        LINEVAL = 240-1 = 0xef
        PAGEWIDTH = 320*4/16 = 0x50
        OFFSIZE = 512 = 0x200
        LCDBANK = 0x0c500000 >> 22 = 0x31
        LCDBASEU = 0x100000 >> 1 = 0x80000
        LCDBASEL = 0x80000 + ( 0x50 + 0x200 ) * ( 0xef + 1 ) = 0xa2b00

Example 2. LCD panel = 320*240, 16gray, dual scan
        Frame start address = 0x0c500000
        Offset dot number = 2048 dots ( 512 half words )

        LINEVAL = 120-1 = 0x77
        PAGEWIDTH = 320*4/16 = 0x50
        OFFSIZE = 512 = 0x200
        LCDBANK = 0x0c500000 >> 22 = 0x31
        LCDBASEU = 0x100000 >> 1 = 0x80000
```

LCDBASEL = 0x80000 + (0x50 + 0x200) * (0x77 + 1) = 0x91580

Example 3. LCD panel = 320*240, color, single scan

Frame start address = 0x0c500000

Offset dot number = 1024 dots (512 half words)

LINEVAL = 240-1 = 0xef

PAGEWIDTH = 320*8/16 = 0xa0

OFFSIZE = 512 = 0x200

LCDBANK = 0x0c500000 >> 22 = 0x31

LCDBASEU = 0x100000 >> 1 = 0x80000

LCDBASEL = 0x80000 + (0xa0 + 0x200) * (0xef + 1) = 0xa7600

例 1： LCD 屏 = 320*240, 16 级灰度, 单扫描

帧起始地址 = 0x0c500000

偏移点数 = 2048 点 (512 个半字)

LINEVAL = 240-1 = 0xef

PAGEWIDTH = 320*4/16 = 0x50

OFFSIZE = 512 = 0x200

LCDBANK = 0x0c500000 >> 22 = 0x31

LCDBASEU = 0x100000 >> 1 = 0x80000

LCDBASEL = 0x80000 + (0x50 + 0x200) * (0xef + 1) = 0xa2b00

例 2： LCD 屏 = 320*240, 16 级灰度, 双扫描

帧起始地址= 0x0c500000

偏移点数= 2048 点 (512 个半字)

LINEVAL = 120-1 = 0x77

PAGEWIDTH = 320*4/16 = 0x50

OFFSIZE = 512 = 0x200

LCDBANK = 0x0c500000 >> 22 = 0x31

LCDBASEU = 0x100000 >> 1 = 0x80000

LCDBASEL = 0x80000 + (0x50 + 0x200) * (0x77 + 1) = 0x91580

例 3： LCD 屏 = 320*240,彩色, 单扫描

帧起始地址 = 0x0c500000

偏移点数 = 2048 点 (512 个半字)

LINEVAL = 240-1 = 0xef

PAGEWIDTH = 320*8/16 = 0xa0

OFFSIZE = 512 = 0x200

LCDBANK = 0x0c500000 >> 22 = 0x31

LCDBASEU = 0x100000 >> 1 = 0x80000

LCDBASEL = 0x80000 + (0xa0 + 0x200) * (0xef + 1) = 0xa7600

RED Lookup Table Register

Register	Address	R/W	Description	Reset Value
REDLUT	0X4D000020	R/W	**STN**: Red lookup table register	0x00000000

REDLUT	Bit	Description	Initial State
REDVAL	[31:0]	These bits define which of the 16 shades will be chosen by each of the 8 possible red combinations. 000 = REDVAL[3:0], 001 = REDVAL[7:4] 010 = REDVAL[11:8], 011 = REDVAL[15:12] 100 = REDVAL[19:16], 101 = REDVAL[23:20] 110 = REDVAL[27:24], 111 = REDVAL[31:28]	0x00000000

红色查找表寄存器

Register	Address	R/W	Description	Reset Value
REDLUT	0X4D000020	R/W	**STN**: 红色查找表寄存器	0x00000000

REDLUT	Bit	Description	Initial State
REDVAL	[31:0]	这些位定义了选择16种色度当中的哪8种红色组合。 000 = REDVAL[3:0], 001 = REDVAL[7:4] 010 = REDVAL[11:8], 011 = REDVAL[15:12] 100 = REDVAL[19:16], 101 = REDVAL[23:20] 110 = REDVAL[27:24], 111 = REDVAL[31:28]	0x00000000

GREEN Lookup Table Register

Register	Address	R/W	Description	Reset Value
GREENLUT	0X4D000024	R/W	**STN**: Green lookup table register	0x00000000

GREENLUT	Bit	Description	Initial State
GREENVAL	[31:0]	These bits define which of the 16 shades will be chosen by each of the 8 possible green combinations. 000 = GREENVAL[3:0], 001 = GREENVAL[7:4] 010 = GREENVAL[11:8], 011 = GREENVAL[15:12] 100 = GREENVAL[19:16], 101 = GREENVAL[23:20] 110 = GREENVAL[27:24], 111 = GREENVAL[31:28]	0x00000000

绿色查找表寄存器

Register	Address	R/W	Description	Reset Value
GREENLUT	0X4D000020	R/W	**STN**: 绿色查找表寄存器	0x00000000

GREENLUT	Bit	Description	Initial State
GREENVAL	[31:0]	这些位定义了选择16种色度当中的哪8种绿色组合。 000 = GREENVAL[3:0], 001 = GREENVAL[7:4] 010 = GREENVAL[11:8], 011 = GREENVAL[15:12] 100 = GREENVAL[19:16], 101 = GREENVAL[23:20] 110 = GREENVAL[27:24], 111 = GREENVAL[31:28]	0x00000000

BLUE Lookup Table Register

Register	Address	R/W	Description	Reset Value
BLUELUT	0X4D000028	R/W	**STN**: Blue lookup table register	0x0000

BULELUT	Bit	Description	Initial State
BLUEVAL	[15:0]	These bits define which of the 16 shades will be chosen by each of the 4 possible blue combinations. 00 = BLUEVAL[3:0], 01 = BLUEVAL[7:4] 10 = BLUEVAL[11:8], 11 = BLUEVAL[15:12]	0x0000

蓝色查找表寄存器

Register	Address	R/W	Description	Reset Value
BLUELUT	0X4D000028	R/W	**STN**: 蓝色查找表寄存器	0x0000

BULELUT	Bit	Description	Initial State
BLUEVAL	[15:0]	这些位定义了选择16种色度当中的哪8种蓝色组合。 00 = BLUEVAL[3:0], 01 = BLUEVAL[7:4] 10 = BLUEVAL[11:8], 11 = BLUEVAL[15:12]	0x0000

NOTE: Address from 0x14A0002C to 0x14A00048 should not be used. This area is reserved for Test mode.

注意：不能使用从 0x14A0002C 到 0x14A00048 的地址空间。这个区域是为测试模式保留的。

Dithering Mode Register

Register	Address	R/W	Description	Reset Value
DITHMODE	0X4D00004C	R/W	**STN**: Dithering mode register. This register reset value is 0x00000 But, user can change this value to 0x12210. (Refer to a sample program source for the latest value of this register.)	0x00000

DITHMODE	BIT	Description	Reset Value
DITHMODE	[18:0]	Use one of following value for your LCD: 0x00000 or 0x12210	0x00000

抖动模式寄存器

Register	Address	R/W	Description	Reset Value
DITHMODE	0X4D00004C	R/W	**STN**: 抖动模式寄存器 此寄存器复位值为0x00000。不过用户可将此值修改为0x12210。 (对于此寄存器的最终值可参考源程序。)	0x00000

DITHMODE	BIT	Description	Reset Value
DITHMODE	[18:0]	根据你的LCD屏，使用下列中的一个值 0x00000或0x12210	0x00000

Temp Palette Register

Register	Address	R/W	Description	Reset Value
TPAL	0X4D000050	R/W	**TFT**: Temporary palette register. This register value will be video data at next frame.	0x00000000

TPAL	Bit	Description	Reset Value
TPALEN	[24]	Temporary palette register enable bit. 0 = Disable 1 = Enable	0
TPALVAL	[23:0]	Temporary palette value register. TPALVAL[23:16] : RED TPALVAL[15:8] : GREEN TPALVAL[7:0] : BLUE	0x000000

临时调色板寄存器

Register	Address	R/W	Description	Reset Value
TPAL	0X4D000050	R/W	**TFT**：临时调色板寄存器。 此寄存器的值为下一帧的视频数据。	0x00000000

TPAL	Bit	Description	Reset Value
TPALEN	[24]	临时调色板寄存器使能位。 0 = 无效 1 = 有效	0
TPALVAL	[23:0]	临时调色板值寄存器。 TPALVAL[23:16] : RED TPALVAL[15:8] : GREEN TPALVAL[7:0] : BLUE	0x000000

LCD Interrupt Pending Register

Register	Address	R/W	Description	Reset Value
LCDINTPND	0X4D000054	R/W	Indicate the LCD interrupt pending register	0x0

LCDINTPND	Bit	Description	Reset Value
INT_FrSyn	[1]	LCD frame synchronized interrupt pending bit. 0 = The interrupt has not been requested. 1 = The frame has asserted the interrupt request.	0
INT_FiCnt	[0]	LCD FIFO interrupt pending bit. 0 = The interrupt has not been requested. 1 = LCD FIFO interrupt is requested when LCD FIFO reaches trigger level.	0

LCD中断挂起寄存器

Register	Address	R/W	Description	Reset Value
LCDINTPND	0X4D000054	R/W	指示LCD中断请求状态	0x0

LCDINTPND	Bit	Description	Reset Value
INT_FrSyn	[1]	LCD帧同步中断请求位 0 = 无中断请求。 1 = 帧已插入中断请求。	0
INT_FiCnt	[0]	LCD FIFO中断请求位。 0 = 无中断请求。 1 = 当 LCD FIFO 达到触发水平时发出中断请求。	0

LCD Source Pending Register

Register	Address	R/W	Description	Reset Value
LCDSRCPND	0X4D000058	R/W	Indicate the LCD interrupt source pending register	0x0

LCDSRCPND	Bit	Description	Reset Value
INT_FrSyn	[1]	LCD frame synchronized interrupt source pending bit. 0 = The interrupt has not been requested. 1 = The frame has asserted the interrupt request.	0
INT_FiCnt	[0]	LCD FIFO interrupt source pending bit. 0 = The interrupt has not been requested. 1 = LCD FIFO interrupt is requested when LCD FIFO reaches trigger level.	0

LCD Interrupt Mask Register

Register	Address	R/W	Description	Reset Value
LCDINTMSK	0X4D00005C	R/W	Determine which interrupt source is masked. The masked interrupt source will not be serviced.	0x3

LCDINTMSK	Bit	Description	Reset Value
FIWSEL	[2]	Determine the trigger level of LCD FIFO. 0 = 4 words 1 = 8 words	
INT_FrSyn	[1]	Mask LCD frame synchronized interrupt. 0 = The interrupt service is available. 1 = The interrupt service is masked.	1
INT_FiCnt	[0]	Mask LCD FIFO interrupt. 0 = The interrupt service is available. 1 = The interrupt service is masked.	1

LCD中断屏蔽寄存器

Register	Address	R/W	Description	Reset Value
LCDINTMSK	0X4D00005C	R/W	决定哪一个中断源被屏蔽。 被屏蔽的中断源将不会被响应。	0x3

LCDINTMSK	Bit	Description	Reset Value
FIWSEL	[2]	决定LCD FIFO的触发水平。 0 = 4 words 1 = 8 words	
INT_FrSyn	[1]	屏蔽LCD帧同步中断。 0 = 中断服务可用。 1 = 中断服务被屏蔽。	1
INT_FiCnt	[0]	屏蔽LCD FIFO中断。 0 = 中断服务可用。 1 = 中断服务被屏蔽。	1

LPC3600 Control Register

Register	Address	R/W	Description	Reset Value
LPCSEL	0X4D000060	R/W	This register controls the LPC3600 modes.	0x4

LPCSEL	Bit	Description	Reset Value
RES_SEL	[1]	1 = 240×320	0
LPC_EN	[0]	Determine LPC3600 Enable/Disable. 0 = LPC3600 Disable 1 = LPC3600 Enable	0

LPC3600控制寄存器

Register	Address	R/W	Description	Reset Value
LPCSEL	0X4D000060	R/W	此寄存器控制LPC3600的模式。	0x4

LPCSEL	Bit	Description	Reset Value
RES_SEL	[1]	1 = 240×320	0
LPC_EN	[0]	LPC3600使能位。 0 = LPC3600 Disable 1 = LPC3600 Enable	0

Register Setting Guide (STN)

The LCD controller supports multiple screen sizes by special register setting.

The CLKVAL value determines the frequency of VCLK. This value has to be determined such that the VCLK value is greater than data transmission rate. The data transmission rate for the VD port of the LCD controller is used to determine the value of CLKVAL register.

The data transmission rate is given by the following equation:

Data transmission rate = HS×VS×FR×MV

HS: Horizontal LCD size
VS: Vertical LCD size
FR: Frame rate
MV: Mode dependent value

Table 15-6. MV Value for Each Display Mode

Mode	MV Value
Mono, 4-bit single scan display	1/4
Mono, 8-bit single scan display or 4-bit dual scan display	1/8
4 level gray, 4-bit single scan display	1/4
4 level gray, 8-bit single scan display or 4-bit dual scan display	1/8
16 level gray, 4-bit single scan display	1/4
16 level gray, 8-bit single scan display or 4-bit dual scan display	1/8
Color, 4-bit single scan display	3/4
Color, 8-bit single scan display or 4-bit dual scan display	3/8

寄存器设置向导（STN）

通过对专用寄存器的设置，LCD 控制器可支持多种尺寸的 LCD 屏

VCLK 的频率由 CLKVAL 的值决定。CLKVAL 的取值应这样决定：必须使 VCLK 的值大于数据传输速率。LCD 控制器中 VD 端口的数据传输速率决定着 CLKVAL 寄存器的值。

数据传输速率由以下议程给出：

数据传输速率 = HS×VS×FR×MV ，其中

HS：LCD 屏的水平尺寸
VS：LCD 屏的垂直尺寸
FR：帧频
MV：模式依赖值

Table 15-6. 各种显示模式下MV的值

模式	MV值
单色，4位单扫描显示	1/4
单色，8位单扫描或4位双扫描显示	1/8
4级灰度，4位单扫描显示	1/4
4级灰度，8位单扫描或4位双扫描显示	1/8
16级灰度，4位单扫描显示	1/4
16级灰度8位单扫描或4位双扫描显示	1/8
彩色，4位单扫描显示	3/4
彩色，8位单扫描或4位双扫描显示	3/8

The LCDBASEU register value is the first address value of the frame buffer. The lowest 4 bits must be eliminated for burst 4 word access. The LCDBASEL register value depends on LCD size and LCDBASEU. The LCDBASEL value is given by the following equation:

LCDBASEL = LCDBASEU + LCDBASEL offset

寄存器 LCDBASEU 的值为帧缓冲区的首地址。The lowest 4 bits must be eliminated for burst 4 word access. 寄存器 LCDBASEL 的值依赖于 LCD 尺寸和 LCDBASEU 的值而确定。LCDBASEL 的值由以下方程给出：

LCDBASEL = LCDBASEU + LCDBASEL 偏移量

Example 1:

160 x 160, 4-level gray, 80 frame/sec, 4-bit single scan display, HCLK frequency is 60 MHz WLH = 1, WDLY = 1.

Data transmission rate = 160×160×80×1/4 = 512 kHz
CLKVAL = 58, VCLK = 517 kHz
HOZVAL = 39, LINEVAL = 159

LINEBLANK =10
LCDBASEL = LCDBASEU + 3200
NOTE: The higher the system load is, the lower the cpu performance is.

Example 2 (Virtual Screen Register):

4 -level gray, Virtual screen size = 1024×1024, LCD size = 320×240, LCDBASEU = 0x64, 4-bit dual scan.

1 halfword = 8 pixels (4-level gray),
Virtual screen 1 line = 128 halfword = 1024 pixels,
LCD 1 line = 320 pixels = 40 halfword,
OFFSIZE = 128 - 40 = 88 = 0x58,
PAGEWIDTH = 40 = 0x28

LCDBASEL = LCDBASEU + (PAGEWIDTH + OFFSIZE)×(LINEVAL +1) = 100 + (40 + 88)×120 = 0x 3C64

例 1：

160 x 160, 4 级灰度, 80 帧/秒, 4 位单扫描显示 HCLK 频率为 60 MHz WLH = 1, WDLY = 1.
数据传输速率 = 160×160×80×1/4 = 512 kHz
CLKVAL = 58, VCLK = 517 kHz
HOZVAL = 39, LINEVAL = 159

LINEBLANK =10
LCDBASEL = LCDBASEU + 3200
注意：系统负担越高，CPU 的表现越差。

例 2：（虚拟屏寄存寄存器）

4 级灰度，虚拟屏尺寸= 1024×1024, LCD 尺寸= 320×240, LCDBASEU = 0x64, 4 位双扫描

1 半字 = 8 个像素 (4 级灰度),
虚拟屏的 1 行 = 128 半字 = 1024 个像素,
LCD 屏的 1 行 = 320 个像素 = 40 个半字,
OFFSIZE = 128 - 40 = 88 = 0x58,
PAGEWIDTH = 40 = 0x28
LCDBASEL = LCDBASEU + (PAGEWIDTH + OFFSIZE)×(LINEVAL +1) = 100 + (40 + 88)×120 = 0x 3C64

Gray Level Selection Guide

The S3C2410X LCD controller can generate 16 gray level using Frame Rate Control (FRC). The FRC characteristics may cause unexpected patterns in gray level. These unwanted erroneous patterns may be shown in fast response LCD or at lower frame rates.

Because the quality of LCD gray levels depends on LCD's own characteristics, the user has to select an appropriate gray level after viewing all gray levels on user's own LCD.

Select the gray level quality through the following procedures:

1. Get the latest dithering pattern register value from SAMSUNG.
2. Display 16 gray bar in LCD.
3. Change the frame rate into an optimal value.
4. Change the VM alternating period to get the best quality.
5. As viewing 16 gray bars, select a good gray level, which is displayed well on your LCD.
6. Use only the good gray levels for quality.

灰度选择向导

利用帧频控制（FRC）S3C2410XLCD 控制器可产生 16 级灰度。帧频控制的特点是可导致意想不到的灰度类型。这些不希望有的错误类型在快速响应的 LCD 上或在比较低的帧速率时可能会显示出来。

因为 LCD 灰度显示的质量依赖于 LCD 本身的特点，用户可先观察 LCD 所有的灰度水平，然后才选择合适的灰度水平。

可通过以下步骤来选择灰度质量。

1. 从 SAMSUNG 获取最新的抖动模式寄存器值。
2. 在 LCD 上显示 16 级灰度条。
3. 修改帧频到最佳值。
4. 改变 VM 交替周期以获得最佳质量。
5. 观察完 16 级灰度条后，可选用在你的 LCD 正常显示的灰度。
6. 只使用质量好的灰度。

LCD Refresh Bus Bandwidth Calculation Guide

The S3C2410X LCD controller can support various LCD display sizes. To select a suitable size (for the flicker free LCD system application), the user have to consider the LCD refresh bus bandwidth determined by the LCD display size, bit per pixel (bpp), frame rate, memory bus width, memory type, and so on.

LCD Data Rate(Byte/s)=bppx(Horizontal display size)x(Vertical display size)x(Frame rate) /8
LCD DMA Burst Count(Times/s)=LCD Data Rate(Byte/s) /16(Byte);LCD DMA using 4words(16Byte) burst

Pdma means LCD DMA access period. In other words, the value of Pdma indicates the period of four-beat burst (4-words burst) for video data fetch. So, Pdma depends on memory type and memory setting.

Eventually, LCD System Load is determined by LCD DMA Burst Count and Pdma.

LCD System Load = LCD DMA Burst Count x Pdma

LCD 自刷新总线带宽计算向导

S3C2410X LCD 控制器可支持各种各样的 LCD 尺寸。

Example 3:

640×480, 8bpp, 60 frame/sec, 16-bit data bus width, SDRAM (Trp=2HCLK / Trcd=2HCLK / CL=2HCLK) and

HCLK frequency is 60 MHz

LCD Data Rate = 8 ×640×480 60 / 8 = 18.432Mbyte/s
LCD DMA Burst Count = 18.432 / 16 = 1.152M/s
Pdma = (Trp+Trcd+CL+(×4)+1×(1/60 MHz) = 0.250ms
LCD System Load = 1.152×250 = 0.288

System Bus Occupation Rate = (0.288/1)×100 = 28.8%

Register Setting Guide (TFT LCD)

The CLKVAL register value determines the frequency of VCLK and frame rate.

Frame Rate = 1/ [{ (VSPW+1) + (VBPD+1) + (LIINEVAL + 1) + (VFPD+1) }×{(HSPW+1) + (HBPD +1) + (HFPD+1) + (HOZVAL + 1) }×{ 2×(CLKVAL+1) / (HCLK) }]

For applications, the system timing must be considered to avoid under-run condition of the fifo of the lcd controller caused by memory bandwidth contention.

寄存器设置向导(TFT LCD)

VCLK 的频率和帧频率由寄存器 CLKVAL 的值决定。

帧频 = 1/ [{ (VSPW+1) + (VBPD+1) + (LIINEVAL + 1) + (VFPD+1) }×{(HSPW+1) + (HBPD +1) + (HFPD+1) + (HOZVAL + 1) }×{ 2×(CLKVAL+1) / (HCLK) }]

实际应用中，由于内存带宽的限制，必须考虑系统的时序，以避免 FIFO 跑空的情况出现。

Example 4:

TFT Resolution: 240 240,
VSPW = 2, VBPD = 14, LINEVAL = 239, VFPD = 4
HSPW = 25, HBPD = 15, HOZVAL = 239, HFPD = 1
CLKVAL = 5
HCLK = 60M (Hz)
The parameters below must be referenced by LCD size and driver specifications:
VSPW, VBPD, LINEVAL, VFPD, HSPW, HBPD, HOZVAL, and HFPD
If target frame rate is 60 - 70Hz, then CLKVAL should be 5.
So, Frame Rate = 67Hz

例 4：

TFT 屏分辨率：240×240
VSPW = 2, VBPD = 14, LINEVAL = 239, VFPD = 4
HSPW = 25, HBPD = 15, HOZVAL = 239, HFPD = 1
CLKVAL = 5
HCLK = 60M (Hz)
下列的参量必须由 LCD 尺寸和驱动器规格参考设定。
VSPW、VBPD、LINEVAL、VFPD、HSPW、HBPD、HOZVAL 和 HFPD
帧频目标值为 60 到 70Hz，则 CLKVAL 的值应为 5，所以帧频为 67Hz。

Known Problems

Problem : In a MDS, such as Multi-ICE, some of the LCD controller registers may be displayed incorrectly in the memory view window of the ARM debugger.

Solution : The LCD controller register will be displayed correctly unless the memory view window is used. Instead, use 'pr' command in the debugger console window.

张杰(whut)于 2007 年 3 月翻译
水平有限，错误之处，敬请指出。
Email: zhjie1983@163.com
QQ：7367427